XVME-244
6U 64-Channel Isolated Digital I/O Module

USER'S MANUAL

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1.1 INTRODUCTION

The XVME-244 Digital I/O module provides VMEbus systems with 64 optically isolated I/O channels, 32 input channels and 32 output channels. The inputs are arranged in four groups of eight each. Each group is optically isolated from the others and from the VMEbus circuitry.

Typical applications for the XVME-244 Digital I/O module include:

Inputs	Outputs
• Limit switches	• Control valves
• Proximity switches	• Alarm interface
• Photo detector switches	• Parallel interface
• Alarm trips	• Indicator lamps

1.2 MANUAL STRUCTURE

The purpose of this first chapter is to introduce the user to the general specifications and functional capabilities of the XVME-244 Digital I/O module. Chapter 2 will develop the various aspects of module installation and operation. Chapter 3 provides the necessary information needed to program the input and output data transfers. The appendices are designed to introduce and reinforce a variety of module-related topics including: Xycom's Standard I/O Architecture, block diagram, and assembly drawings.

Chapter One - A general description of the XVME-244 Digital I/O module, including complete functional and environmental specifications, VMEbus compliance information, and a block diagram.

Chapter Two - Module installation information covering the location of pertinent module components, switch and jumper options, external connector pin locations and standard board installation information.

Chapter Three - Provides information needed to program the input and output data transfers

Appendix A - Xycom standard I/O architecture

Appendix B - Block diagram, assembly drawing, and schematics

1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows an operational block diagram of the XVME-244 Digital I/O module.

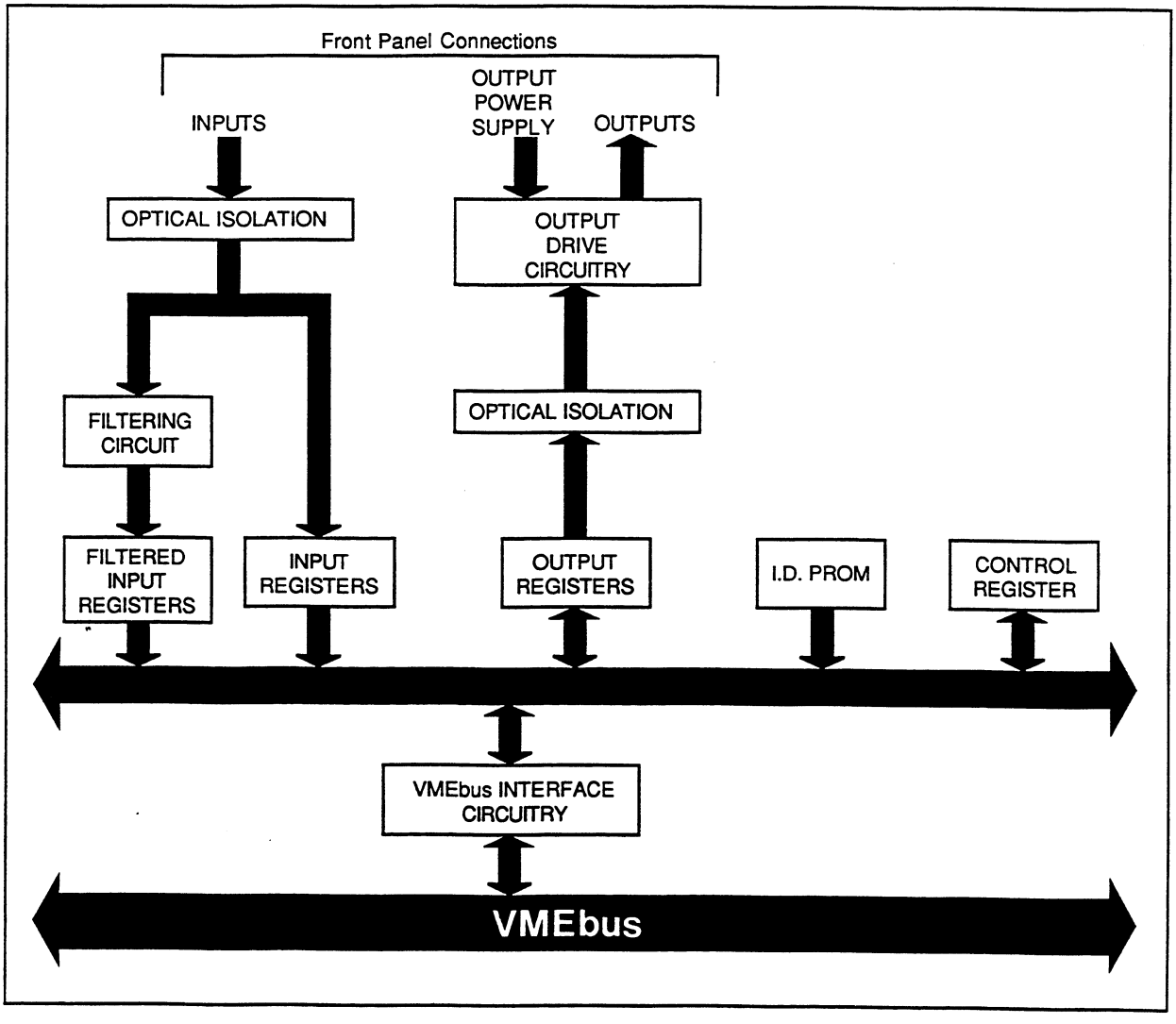


Figure 1-1. XVME-244 Digital I/O Module Operational Block Diagram

1.4 SPECIFICATIONS

The following Table (which is continued on page 1-4) is a list of operational and environmental specifications for the XVME-244 Digital I/O module.

Table l-l. XVME-244 Digital I/O Module Specifications

CHARACTERISTIC	SPECIFICATION
OUTPUTS	
Number of channels	32 (4 groups of 8)
Configuration	Current sourcing outputs
Power supply voltage range	l0-15 VDC or 15-30 VDC, jumper selectable
On-state output voltage	(V supply - 0.8V) min.
Power supply ground current	35 mA max.
Off-state leakage current	400 uA max.
On-state output current	400 mA max.
Turn-on time	10 usec max.
Turn-off time	120 usec max.
Transient Protection	
Reverse voltage protection and transient suppression provided	
INPUTS	
Number of channels	32 (4 groups of 8)
Input Voltage Range	-35to +35
Logic 1	10 to 35 VDC
Logic 0	-35 to 3 VDC
Typical threshold voltage	6 VDC
Input Current Range	0to14 mA
Logic 1	2.3 mA to 14 mA
Logic 0	0 to 400 μA
Typical threshold current	1.1 mA
Input Impedance	2.5 kΩmin
Input Propagation Delay	
Off-to-on	30 usec worst case
On-to-off	175 usec worst case
Input Debounce Time	12 ± 3 ms
Maximum Input Frequency	2.8 KHz
Isolation	
Any I/O group to any I/O group	300 VDC
Any I/O group to VMEbus	1000 VDC
Power Requirements	+5V @ 1.0 A typical
	+5V @ 1.2 A max.

Table 1-1. XVME-244 Digital I/O Module Specifications (Continued)

CHARACTERISTIC	SPECIFICATION
Environmental	
Temperature	
Operating	0° to 65° C (32° to 149° F)'
Non-operating	-40° to 85° C (-40" to 185° F)
Humidity	5 to 95% RH, non-condensing
Altitude	
Operating	Sea level to 10,000 ft. (3048 m)
Non-operating	Sea level to 50,000 ft. (15240 m)
Vibration	
Operating	.015" peak to peak 2.5 g peak acceleration
Non-operating	.030" peak to peak 5.0 g peak acceleration
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-operating	50 g peak acceleration, 11 msec duration

VMEbus Compliance

Complies with VMEbus specification, IEEE 1014, Rev. C.l

- A24/A16:Dl6/D08(EO) DTB slave
- Utility signals - SYSFAIL
- Form factor: DOUBLE 233.35 mm x 160 mm (9.2" x 6.3)
- Conforms to Xycom Standard I/O Architecture

***CAUTION**

A fan rated at 40 CFM minimum should be used. Forced air is not required in systems where the voltage on all inputs will not exceed 30 VDC. Forced air is also not required in systems which limit the ambient temperature of the module to 40°C.

2.1 INTRODUCTION

This chapter explains how to configure the XVME-244 Digital I/O module prior to installation in a VMEbus system. Included in this chapter is information on the jumper options, the jumper locations, switch options, switch locations, and external connector pin descriptions.

2.2 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers and switches on the XVME-244 Digital I/O Module are illustrated in Figure 2-1 below.

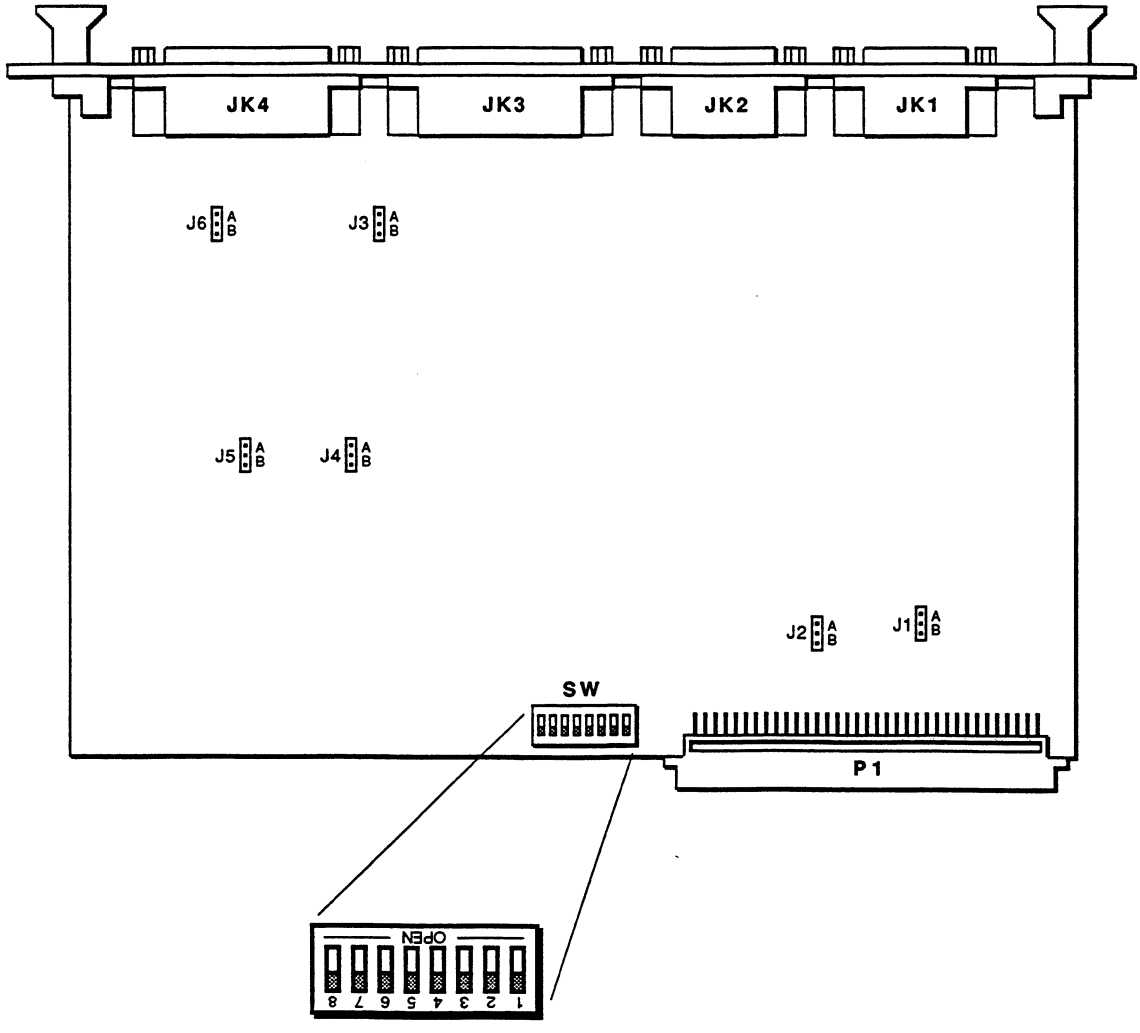


Figure 2-1. Location of Jumpers, Switches, Sockets, and Connectors

2.2.1 Selecting the Module Base Address

All module registers reside in the VMEbus short I/O memory space or the upper 64Kbyte space of the standard (A24) memory space. The module is switch selectable, via SW1, to occupy a particular 1K block of memory space. Figure 2-2 shows Switch 1 pole assignments.

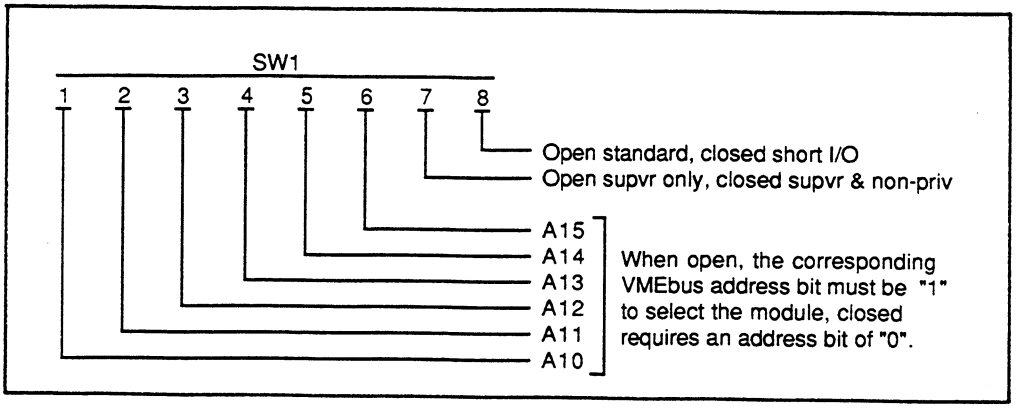

SW1
1 2 3 4 5 6 7 8
Open standard, closed short I/O
Open supvr only, closed supvr & non-priv
A15
A14
A13
A12
A11
A10
When open, the corresponding VMEbus address bit must be "1" to select the module, closed requires an address bit of "0".

Figure 2-2. Switch 1/ Eight Pole Switch Assignments

Switch 1 bit 8 is used to select between VMEbus short I/O or standard memory spaces. When the standard memory space is selected, the upper eight address bits must be 0ffh. The lower six positions of SW1 determine which one of the 64 1Kbyte boundaries will be occupied. The module occupies 256 bytes in these spaces.

2.2.2 SYSFAIL Operation

There are two jumper options which govern the module's interaction with SYSFAIL. Each is a two position jumper designated as A and B.

J2 will allow the module to assert SYSFAIL when the FAIL LED is on. When J2 is in the A position, the module will assert SYSFAIL when the FAIL LED is on. When J2 is in the B position, the module will never assert SYSFAIL.

J1 chooses whether to clear the output registers in response to the assertion of SYSFAIL. When J1 is in the A position, the output registers will reset to zero when SYSFAIL is asserted. The output registers cannot be set to a one state until SYSFAIL is negated. When J1 is in the B position, the state of SYSFAIL has no effect on the output registers.

NOTE

The output registers cannot be set to a one state until SYSFAIL is negated. When Jl is in the B position, the state of SYSFAIL has no effect on the output registers

2.2.3 Output Power Supply Selection

Each output group has a jumper with which to select the power supply voltage range, (refer to Figure 2-3 which shows the mapping of the output signals to the connector pins). When the jumper is in the A position the voltage range is 15-30V. When the jumper is in the B position the range is 10-l 5V. The power voltage should not go below the selected range as this could cause damage to the output channel. Likewise, the power voltage should not exceed the selected range as this could cause the group's fuse to blow. Table 2-1 shows jumpers and their output group.

Table 2-1. Jumper Output Groups

JUMPER	POSITION		GROUP
J4	A 15-30	B l0-15	1
J3	A 15-30	B l0-15	2
J5	A 15-30	B l0-15	3
J6	A 15-30	B l0-15	4

Vcc is monitored by a precision voltage comparator. Discrete circuitry will not allow the outputs to turn on unless Vcc is within operational limits. When Vcc reaches its operational limits, SYSRESET* will have reset the output registers to 0 and the outputs will not turn on.

The outputs are guaranteed to stay off during the application of external power. When external power is being applied and either a 0 is written to the output register or the VMEbus side is not powered on, the outputs will not turn on.

In cases where the VMEbus side is powered up and l's are written to the output registers, the external power supply should rise within a couple of seconds. This will prevent the output transistors from lingering in the linear state and dissipating excessive power.

Group 1		Group 2	
Signal	**Connector-Pin**	**Signal**	**Connector-Pin**
CH0	JK3-30	CH8	JK3-7
CH1	JK3-15	CH9	JK3-6
CH2	JK3-14	CH10	JK3-5
CH3	JK3-13	CH11	JK3-4
CH4	JK3-12	CH12	JK3-3
CH5	JK3-11	CH13	JK3-2
CH6	JK3-10	CH14	JK3-1
CH7	JK3-9	CH15	JK3-16
PWR	JK3-25	PWR	JK3-17
PWR	JK3-26	PWR	JK3-18
PWR	JK3-44	PWR	JK3-34
PWR	JK3-41	PWR	JK3-35
PWR	JK3-42	PWR	JK3-36
PWR	JK3-43	PWR	JK3-19
PWR	JK3-38	PWR	JK3-31
PWR	JK3-39	PWR	JK3-32
PWR	JK3-40	PWR	JK3-33
GND	JK3-28	GND	JK3-21
TEST	JK3-29	TEST	JK3-22
Power supply jumper: J4		Power supply jumper: J3	
Group 3		**Group 4**	
Signal	**Connector-Pin**	**Signal**	**Connector-Pin**
CH16	JK4-30	CH24	JK4-7
CH17	JK4-15	CH25	JK4-6
CH18	JK4-14	CH26	JK4-5
CH19	JK4-13	CH27	JK4-4
CH20	JK4-12	CH28	JK4-3
CH21	JK4-11	CH29	JK4-2
CH22	JK4-10	CH30	JK4-1
CH23	JK4-9	CH31	JK4-16
PWR	JK4-25	PWR	JK4-17
PWR	JK4-26	PWR	JK4-18
PWR	JK4-44	PWR	JK4-34
PWR	JK4-41	PWR	JK4-35
PWR	JK4-42	PWR	JK4-36
PWR	JK4-43	PWR	JK4-19
PWR	JK4-38	PWR	JK4-31
PWR	JK4-39	PWR	JK4-32
PWR	JK4-40	PWR	JK4-33
GND	JK4-28	GND	JK4-21
TEST	JK4-29	TEST	JK4-22
Power supply jumper: J5		Power supply jumper: J6	

Figure 2-3. Output Pin Assignments

2.2.4 Output Connectors

The outputs are accessed through two 44-pin high-density D subminiature connectors (JK3 and JK4). Each connector provides access to two output groups. Figure 2-4 shows the pin definition of these connectors. (Refer to Figure 2-3 for output signal information).

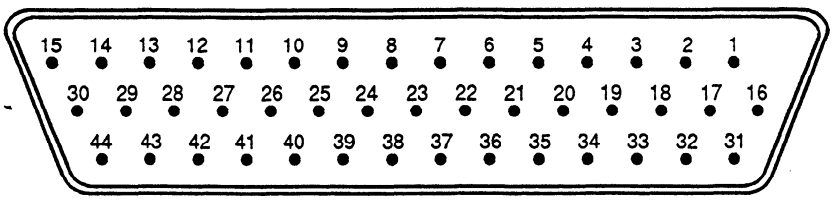


Figure 2-4. Front View of 44 Pin D Subminiature Connector

Each group requires 19 pins:

8	Output signals
1	Test signal
9	Power supply (all tied together)
1	Power supply ground reference

When an output is turned on, current will flow from the power supply pins and come out through the output pin. See Figure 2-5.

When an output is turned off, a small (leakage) current will try to flow out of the output. This will raise the potential of the output to the power supply voltage level (if there is no load on the output). The test signal provides a bias which may be used as a pulldown resistor for system level debugging. When this is connected to an output, the output will assume the ground potential when it is turned off.

The test signal may also be used to test the state of the power fuse for that particular group. If the resistance between the test and ground pins is less than l0K, then the fuse is intact. If the reading is greater than l0K, then the fuse has been blown and needs to be replaced.

There are nine power pins per group. The pins are all connected together on the board. The current supplied from the output pins is drawn from these power pins. The number of power pins depends on the total current supplied through that group's outputs. The current should be limited to a maximum of one ampere per pin. Use this limitation to select the number of power pins to be used in a given application. For example, if each output within a group may source 400 mA, a total of 3.2 amperes will be required from the power supply. In this case, a minimum of four power pins should be used. A total of nine power pins are provided to allow more wire connections in order to decrease the voltage drop across the power supply wires. When excessive voltage drop is experienced, more connections can be made (to a maximum of nine).

Special consideration should be given to the ground connection. This pin requires very little current (voltage drop will be minimal, even with small wires). This connection should connect to the power supply directly (**not to the ground connection of the load**). This will isolate the module from any voltage drop across the load ground wires. See Figure 2-5.

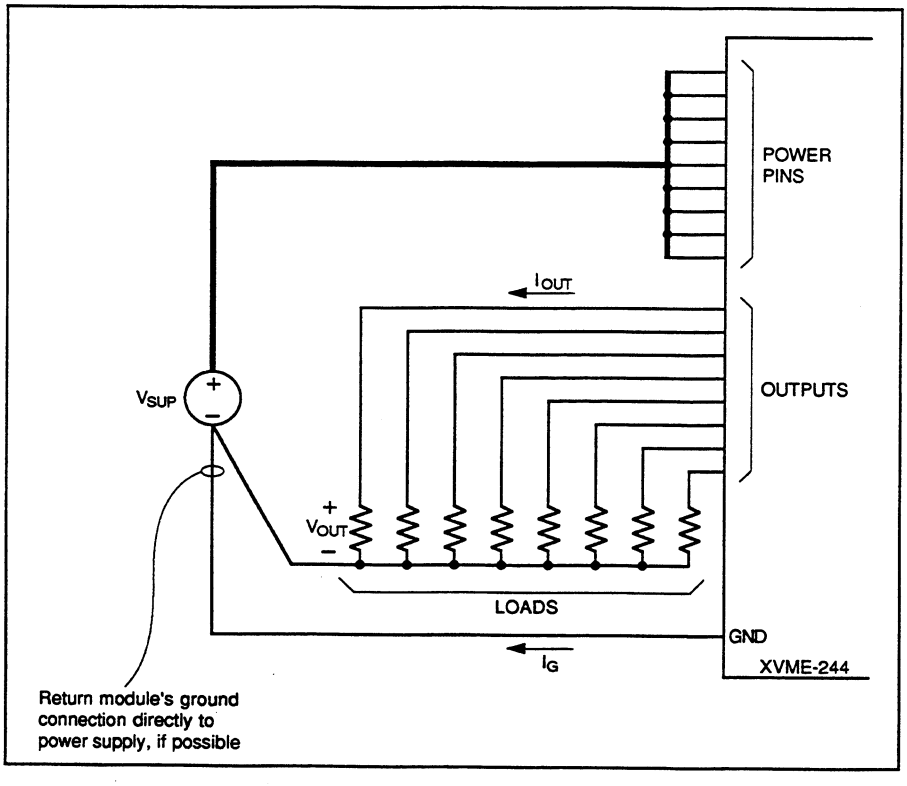


Figure 2-5. Output Group Connection Diagram

2.2.5 Input Connectors

The inputs are accessed through two 26-pin high-density D subminiature connectors (JK1 and JK2). Each connector provides access to two input groups. See Figure 2-6 for the pin definition of these connectors.

There are two ground signals per group. These signals are connected together on the board. Either one or both may be used. The current returned through the ground pins can easily be accommodated by one pin. See Figure 2-7 for the input group connection diagram, and see Figure 2-8 for pin assignments.

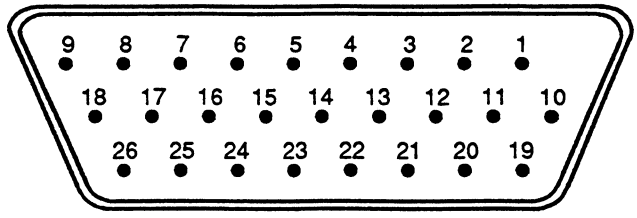


Figure 2-6. Front View of 26 Pin D Subminiature Connector

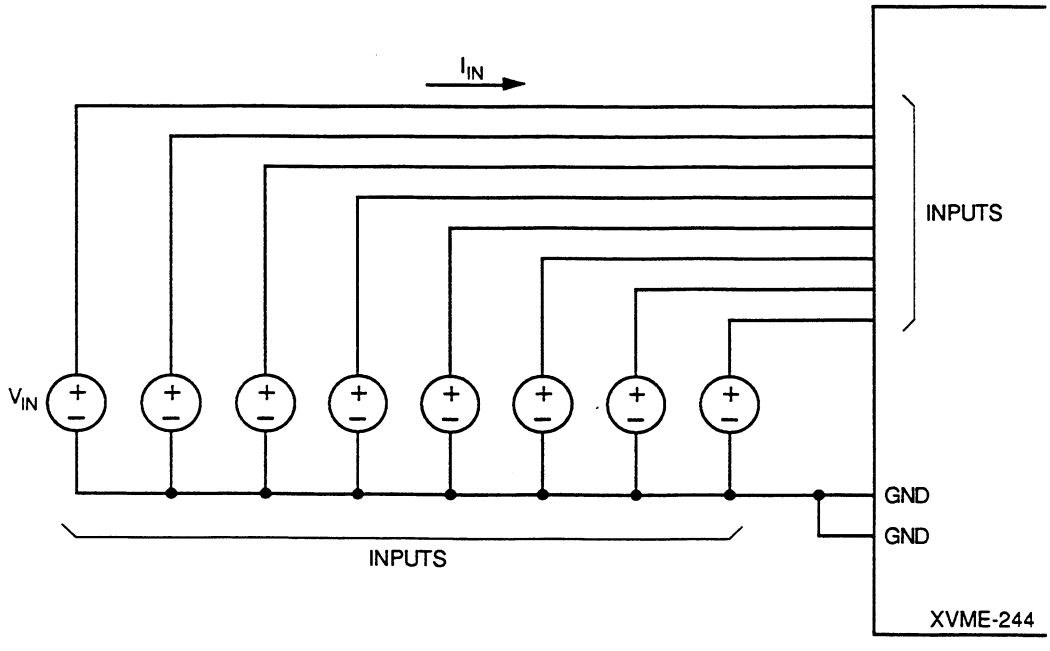


Figure 2-7. Input Group Connection Diagram

Group 1		Group 2	
Signal	**Connector-Pin**	**Signal**	**Connector-Pin**
CH0	JK1-15	CH8	JK1-10
CH1	JK1-6	CH9	JK1-1
CH2	JK1-16	CH10	JK1-11
CH3	JK1-7	CH11	JK1-2
CH4	JK1-17	CH12	JK1-12
CH5	JK1-8	CH13	JK1-3
CH6	JK1-18	CH14	JK1-13
CH7	JK1-9	CH15	JK1-4
GND	JK1-25	GND	JK1-19
GND	JK1-26	GND	JK1-20
Group 3		**Group 4**	
Signal	**Connector-Pin**	**Signal**	**Connector-Pin**
CH16	JK2-15	CH24	JK2-10
CH17	JK2-6	CH25	JK2-1
CH18	JK2-16	CH26	JK2-11
CH19	JK2-7	CH27	JK2-2
CH20	JK2-17	CH28	JK2-12
CH21	JK2-8	CH29	JK2-3
CH22	JK2-18	CH30	JK2-13
CH23	JK2-9	CH31	JK2-4
GND	JK2-25	GND	JK2-19
GND	JK2-26	GND	JK2-20

Figure 2-8. XVME-244 Input Pin Assignments

2.2.6 Using the Inputs to Monitor the Outputs

Since the inputs are electrically compatible with the outputs, the inputs can be connected to the outputs. This is beneficial in situations where the actual state of the output at the connector must be monitored for reliability reasons.

The actual state of the outputs may differ from the output register image. The following lists several reasons:

- Power supply may fail, providing marginal power or no power
- A short may exist in the system, such that the output cannot turn on or off
- Output circuitry's fuse may have blown
- Hardware failure may have occurred on a particular output

By connecting the inputs to the outputs, the outputs'states at the connectors may be monitored through the inputs and these fault conditions can be detected. Figure 2-9 shows the input and output diagram.

NOTE
There is no minimum load requirement when the inputs are used to monitor'the outputs.

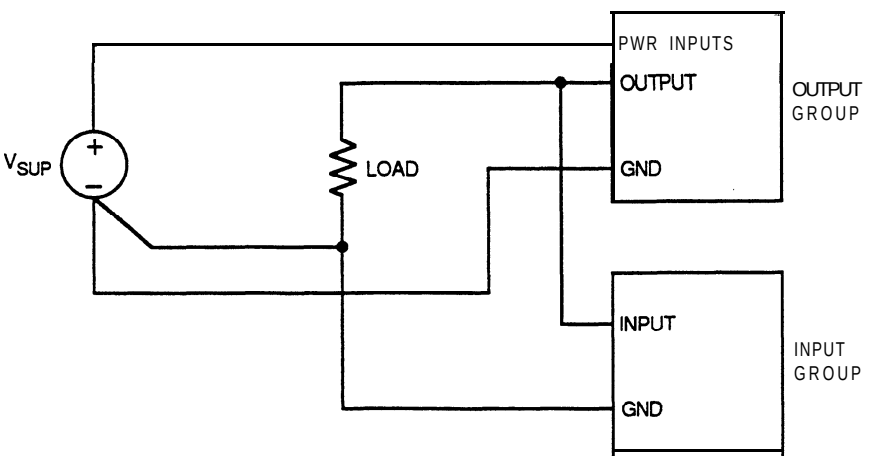


Figure 2-9. Input Monitoring Output Connection Diagram

3.1 INTRODUCTION

This chapter provides the information needed to program the input and output data transfers and how to use the unique design features which are part of Xycom I/O modules.

3.2 MODULE MEMORY MAP

All address references are offsets which are added to the base address selected by SW1 to form the VMEbus address. The memory map of the module is shown in Figure 3-1.

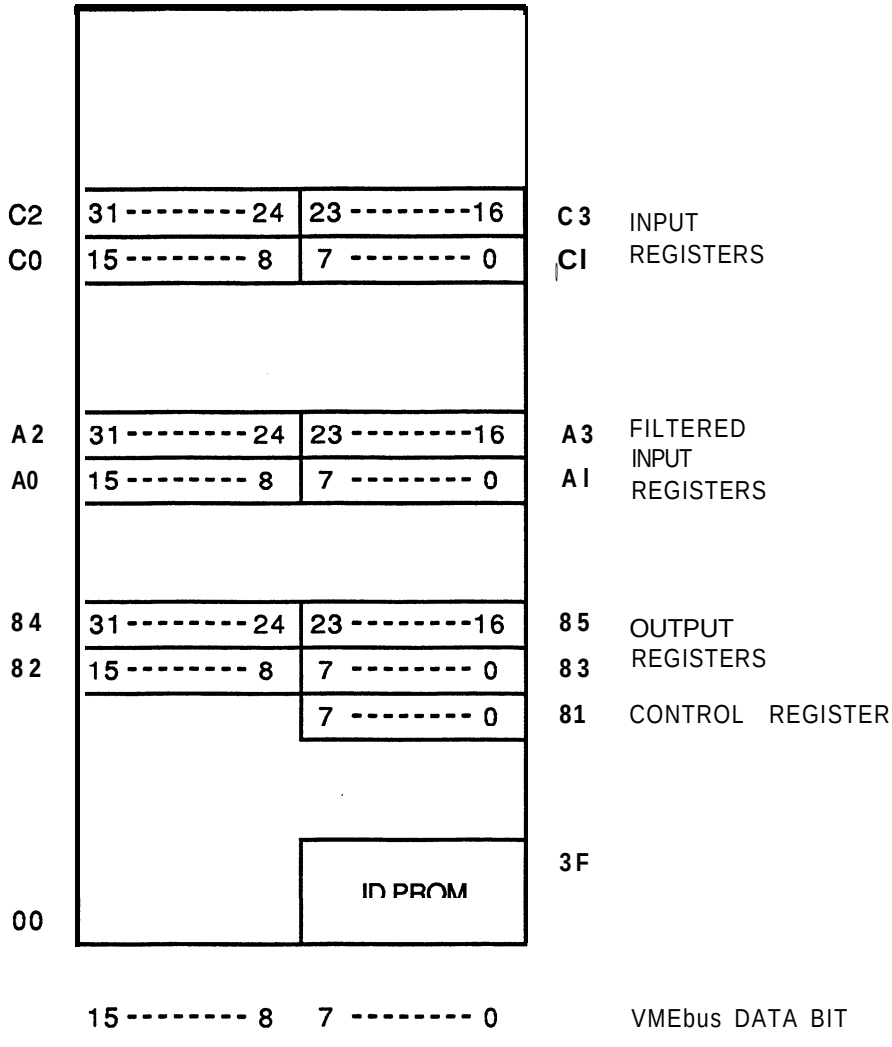


Figure 3-1. Memory Map for XVME-244

3.3 MODULE REGISTERS

The following sections describe the XVME-244 registers residing in the VMEbus short I/O memory space or the upper 64 Kbytes of the standard memory space.

3.3.1 Control Register (Base Address +8lH)

An eight bit read/write control register is provided to control module functions. Two bits control the state of the PASS and FAIL LEDs on the front panel. One bit enables the outputs, while the remaining bits may be used as read/write bits and do not affect module operation. In response to SYSRESET, all output control register bits will go to 0. This will turn the FAIL LED on, turn the PASS LED off, and enable the outputs.

The control register is located at offset 8 IH and has the following format:

Bit 0 (LSB)	0	Will assert SYSFAIL (if J2 is in A position) and turn the FAIL LED on.
	1	Will negate SYSFAIL and turn the FAIL LED off.
Bit 1	0	Will turn the PASS LED off.
	1	Will turn the PASS LED on.
Bit 4	**0**	Will negate the clear condition of the output registers.
	1	Will clear all output registers which forces the outputs off.

NOTE

If Bit 4 is 1 when writing to the output registers, the registers will not accept the data.

3.3.2 ID PROM (Base Address)

A 32 byte PROM is provided containing module identification information. This data is available in odd bytes only. See Figure 3-2 for contents of ID PROM. Refer to Appendix A for definitions of these bytes.

Offset Address	Contents Hex	Contents ASCII
01	56	V
03	4D	M
05	45	E
07	49	I
09	44	D
OB	58	X
OD	59	Y
OF	43	C
11	32	2
13	34	4
15	34	4
17	20	
19	20	
1B	20	
1D	20	
1F	31	1
21	20	
23	31	1
25	31	1
27	20	
29 - 3F	00	

Figure 3-2. ID PROM Contents

3.3.3 Output Registers (Base Address + 82h - 85h)

Four read/write output registers are provided, one for each output group. During reads, the image of the outputs is provided, and a zero bit indicates that its corresponding output is *off,* and a one ***bit*** indicates that it is on. All four registers are forced to zero upon the assertion of SYSRESET, by setting bit 4 of the control register, or by the assertion of SYSFAIL (if Jl is in the A positon). These registers may be accessed as bytes or 16 bit words. See Figure 3-1.

3.3.4 Input Registers (Base Address + Clh - C3h)

Four input registers are provided, one for each group. These registers are read only, providing instantaneous state of the inputs. A zero bit indicates that the corresponding input is *off,* and

a *one* indicates that it is *on*. SYSRESET will have no effect on these registers. These registers may be accessed as bytes or 16 bit words. See Figure 3-1.

3.3.5 Filtered Input Registers (Base Address + Alh - A3h)

The inputs are filtered by circuitry which will eliminate contact intermittency (bounce). This will filter out the bouncing signals typical of mechanical switches. The input needs to switch to a new state and stay in that state for 12 (± 3) mSec before the new state is passed to the filtered input registers. If filtering is desired for a particular input, the filtered input register should be used.

Four filtered input registers are provided, one for each input group. These registers are read only, providing the state of the filtered inputs. A *zero* bit indicates that the corresponding input is *off*, and a *one* indicates that it is *on*. SYSRESET will have no effect on these registers. These registers may be accessed as bytes or 16 bit words. See Figure 3-1.

APPENDIX A - XYCOM STANDARD I/O ARCHITECTURE

A.1 INTRODUCTION

The purpose of this appendix is to define Xycom's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all Xycom XVME I/O modules in offer to provide a simpler and more consistent method of programming for the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the Xycom I/O Architecture are the following:

- **Module Addressing** - Where a module is positioned in the I/O address space and how software can read from it or write to it.
- **Module Identification** - How software can identify which modules are installed in a system.
- **Module Operational Status** - How the operator can (through software) determine the operational condition of specific modules within the system.
- **Interrupt Control** - How software is able to control and monitor the capability of the module to interrupt the system.
- **Communication Between Modules** - How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the I/O modules.
- **I/O Kernel** - How intelligent and non-intelligent "kernels" facilitate the operation of all Xycom I/O modules.

A.2 MODULE ADDRESSING

All Xycom I/O modules are designed to be addressed within the VMEbus-defined 64K short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while at the same time, providing 64K of address space for I/O modules.

A.2.1 Base Addressing

Since an I/O module connected to the bus must have its own unique base address, the base addressing scheme for Xycom VME I/O modules has been designed to be jumper selectable. Each XVME I/O module installed in the system requires at least a IK byte block of the short I/O memory. This divides the 64K short I/O address space into 64 1K segments. Thus, each I/O module has a base address which starts on a 1K boundary. As a result, the Xycom I/O modules have all been implemented to decode base addresses in 1K (400H) increments. On an intelligent XVME module, only address signals AI0-A13 are decoded, while A14 and Al 5 must be zero. (This implies that only the lowest 16 of the possible 64 1K segments are used for

intelligent I/O modules). On non-intelligent XVME modules, the six highest order short I/O address bits are decoded, while the remaining lower order bits are ignored. This arrangement provides the correct address configuration to allow each module address to begin on a IK boundary. Non-intelligent XVME modules allow the use of six base address jumpers (representing bits Al0-A15), therefore, they are able to reside on any of the 64 1K boundaries available in the short I/O address space. Intelligent XVME modules will only allow the use of four base address jumpers (representing bits A10-Al 3) which limit their selection of 1K boundaries to one of sixteen possible choices.

Figure A-l shows an abbreviated view of the short I/O memory.

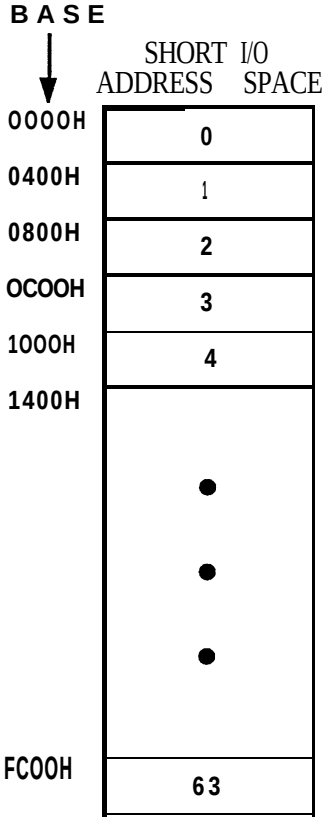


Figure A-l. 64K Short I/O Address Space

A.2.2 Standardized Module I/O Map

The IK block of short I/O addresses (called the I/O Interface Block) allocated to each XVME module is mapped with a standardized format in order to simplify programming and data access. The locations of frequently used registers and module-specific identification information are uniform. For example, the module identification information is always found in the first 32 odd bytes of the module memory block; with these addresses being relative to the jumpered base address (i.e., Module I.D. data address = base address + odd bytes 1H - 3FH). The byte located at base address + 81H on each module contains a Status/Control register which provides the results of diagnostics for verification of the module's operational condition. The remainder of the I/O Interface Block (base address + 82H - 3FFH) is module-specific and it varies in size from one module to the next. It is in this area that the module holds specific registers, buffers, I/O status, data and pointer registers, etc. All intelligent XVME I/O modules have an area of their I/O Interface Blocks defined as "dual access RAM." This area of memory provides the space where XVME "slave" I/O modules access their command blocks and where XVME "master" modules could access their command blocks (i.e., "master" modules can also access global system memory).

Figure A-2, on the following page, shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. Notice that any location in the I/O Interface Block may be accessed by simply using the address formula:

Module Base Address + Relative Offset = Desired Location

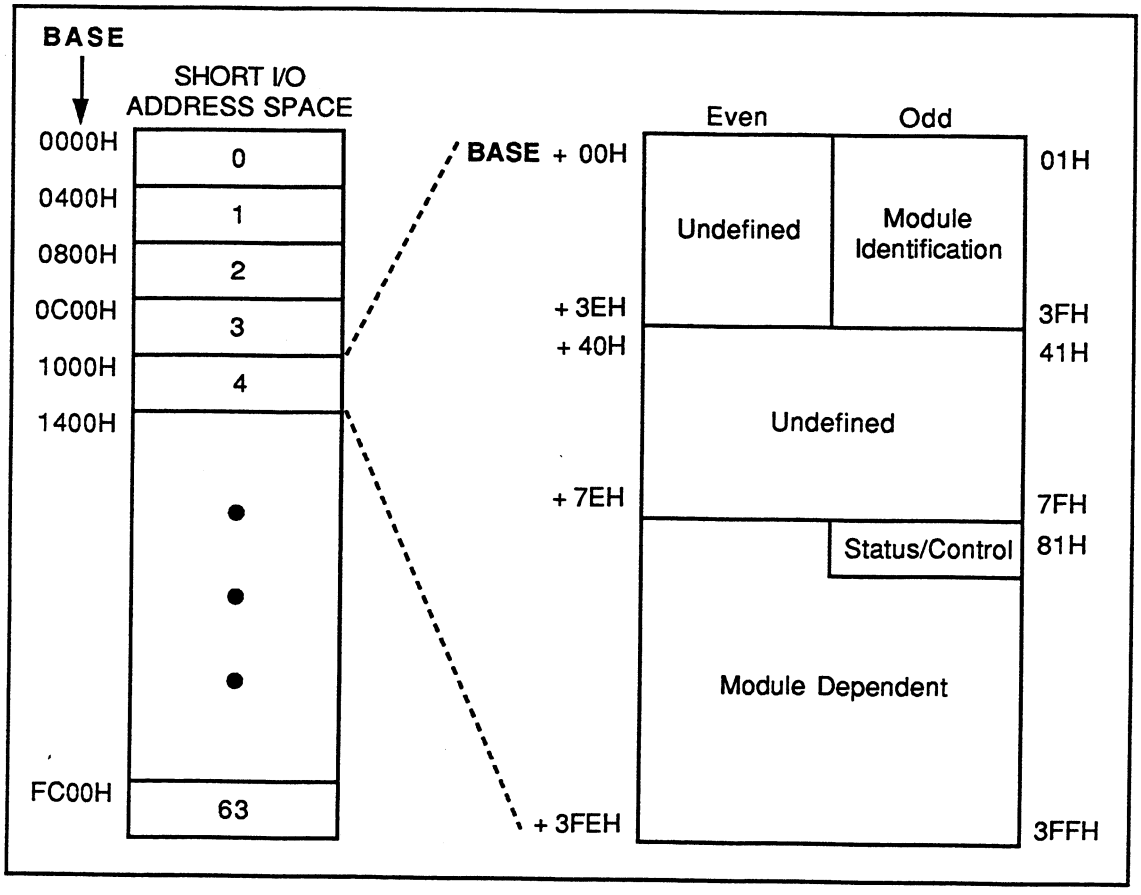


Figure A-2. XVME I/O Module Address Map

A.3 MODULE SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1 Kbyte blocks occupied by the module, and model functional revision level information. This information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1 defines the identification information locations.

Table A-l. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	ID PROM identifier, always "VMEID" (5 characters)
3	M	4D	
5	E	45	
7	1	49	
9	D	44	
B	X	58	Manufacturer's I.D., always "XYC" for XYCOM modules (3 characters)
D	Y	59	
F	C	43	
11	2	32	Module Model Number (3 characters and 4 trailing blanks)
13	4	34	
15	4	34	
17		20	
19		20	
1B		20	
1D		20	
1F		31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision level with leading blank (if single digit)
23	1	31	
25		31	Minor functional revision level with trailing blank (if single digit)
27	1	20	
29			
2B	Undefined		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer Dependent Information, Reserved for future use
37	"		
39	"		
3B	"		
3D	"		
	"		
	"		

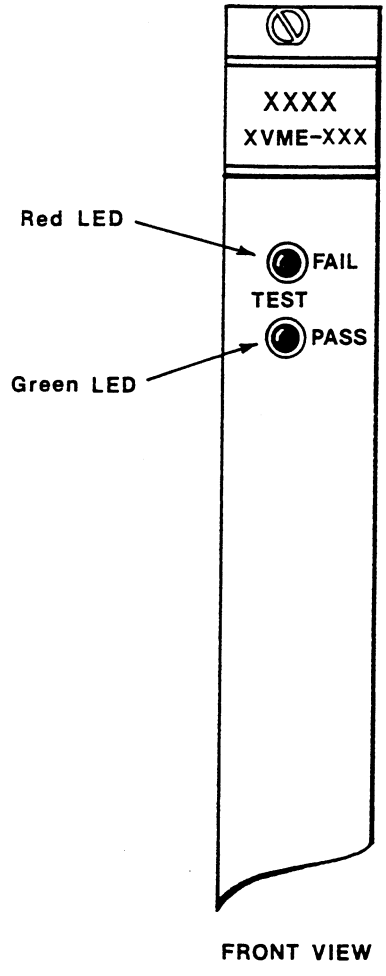
The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. However, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes lH-3FH).

I.D. information can be accessed simply by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to l000H, and if you wish to access the module model number (I/O interface block locations 11 H, 13H, 15H, 17H, 19H, lBH, and IDH), you will individually add the offset address to the base address to read the hex-coded ASCII value at each location. In this example, the ASCII values which make up the module model number are found sequentially at locations 101 IH, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH within the system's short I/O address space.

A.4 MODULE OPERATIONAL STATUS/CONTROL

All XVME intelligent I/O modules are designed to perform diagnostic self-tests on power-up or reset. For non-intelligent modules, the user must provide the diagnostic program. The self-test provision allows the user to verify the operational status of a module by either visually inspecting the two LEDs which are mounted on the module front panel (see Figure A-3) or by reading the module status byte, located at module base address + 81H.

Figure A-3 shows the location of the status LEDs on the module front panel. The two tables included with Figure A-3 define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module passed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

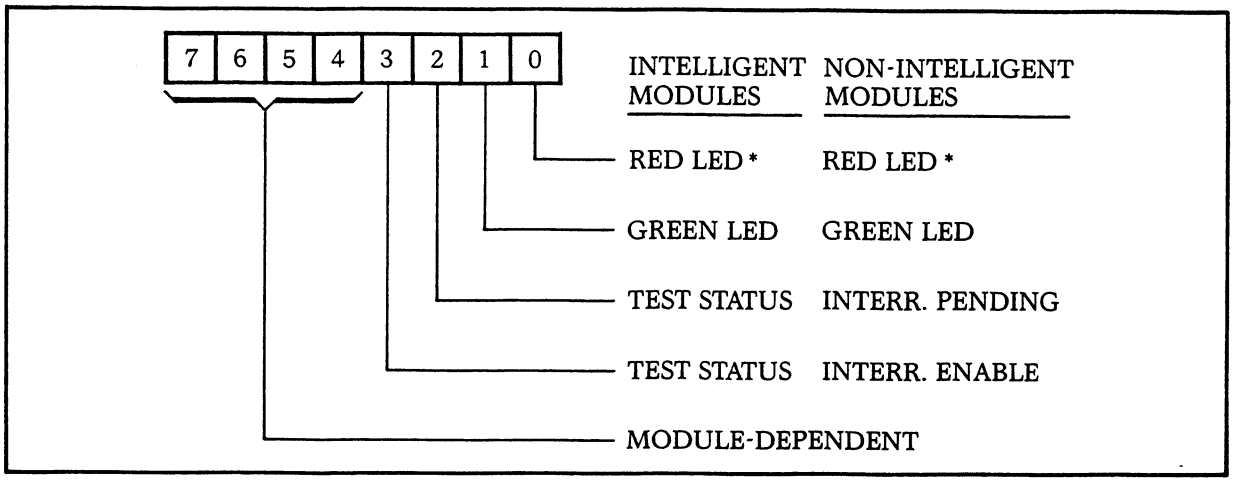
NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

The module status/control register (found at module base address + 8lH) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent module is a "Read Only" register and it can be read by software to determine if the board is operating properly.

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module-generated interrupts. The LED status bits are "Read/Write" locations which provide the user with the indicators to accommodate diagnostic software. The Interrupt Enable bit is also a Read/Write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a "Read Only" bit which indicates a module-generated pending interrupt.

Figure A-4, on the following page, shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules	Bit	Intelligent Modules
0	Read/Write - Red LED 0 = Red LED On 1 = Red LED Off	0	Read Only - Red LED 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On	1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending	2 & 3	Read Only - Test Status Indicators **Bit 3 Bit 2** 0 0 = Self-test not started 0 1 = Self-test not started 1 0 = Self-test failed 1 1 = Self-test passed
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled		
4	Module dependent	4	Module dependent
5	Module dependent	5	Module dependent
6	Module dependent	6	Module dependent
7	Module dependent	7	Module dependent

Figure A-4. Status Register Bit Definitions

A.5 INTERRUPT CONTROL

Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status of pending on-board interrupts can also be read from this register. Interrupt control for intelligent modules is handled by the Interprocessor Communications Protocol.

A.5.1 Communications Between Processors

Communications between an intelligent "master" and an intelligent "slave" I/O module is governed by Xycom's Interprocessor Communication (IPC) Protocol. This protocol involves the use of 20-byte Command Block data structures, which can be located anywhere in shared global RAM or dual-access RAM on an I/O module, to exchange commands and data between a host processor and an I/O module. Interprocessor Communication Protocol is thoroughly explained in Chapter 3 of this manual.

A.6 KERNEL

To standardize its XVME I/O modules, Xycom has designed them around "kernels" common from module to module. Each different module type consists of a standard kernel, combined with module-dependent application circuitry. Module standardization results in more efficient module design and allows the implementation of the Standard I/O Architecture. The biggest benefit of standardization for intelligent modules is that it allows the use of a common command language or protocol (Interprocessor Communication Protocol in this case).

The intelligent kernel is based around a 68000 microprocessor. This design provides the full compliment of VMEbus Requester and Interrupter options for master/slave interfacing, as well as all of the advantages provided by the various facets of the Xycom Standard I/O Architecture (as covered earlier in this appendix).

The non-intelligent kernel provides the circuitry required to receive and generate all of the signals for a VMEbus defined 16-bit "slave" module. The non-intelligent kernel also employs the features of the Xycom Standard I/O Architecture (as described earlier in this Appendix).

On the following page, simplified diagrams (Figure A-5) show the features of both the intelligent and the non-intelligent kernels.

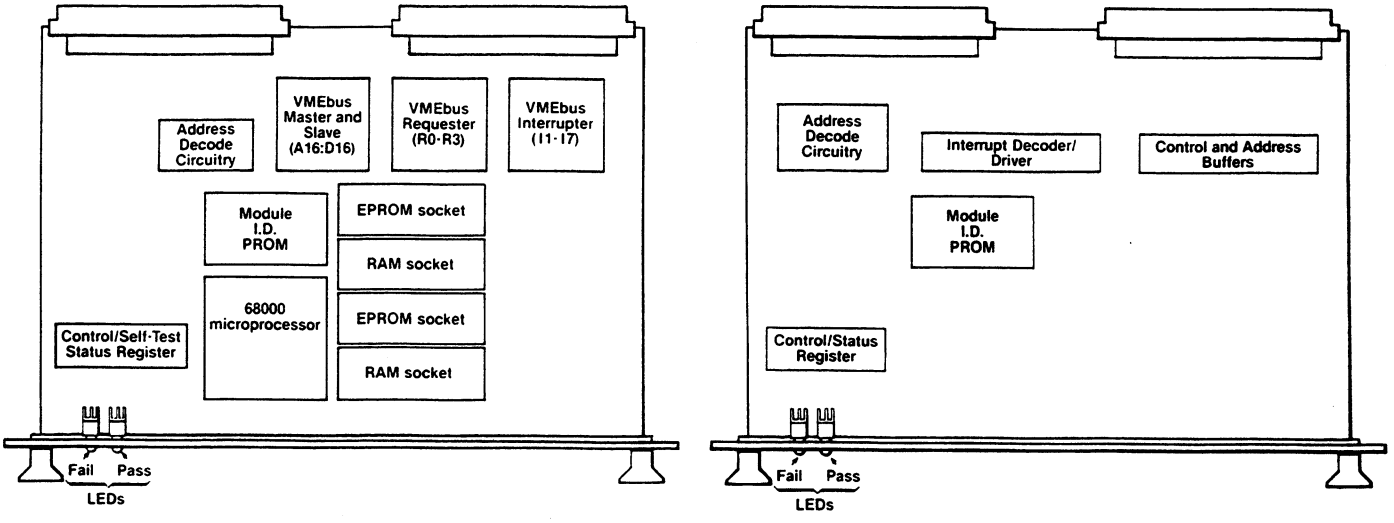


Figure A-5. Intelligent and Non-Intelligent Kernels

APPENDIX B - BLOCK DIAGRAM, ASSEMBLY DRAWING, AND SCHEMATICS

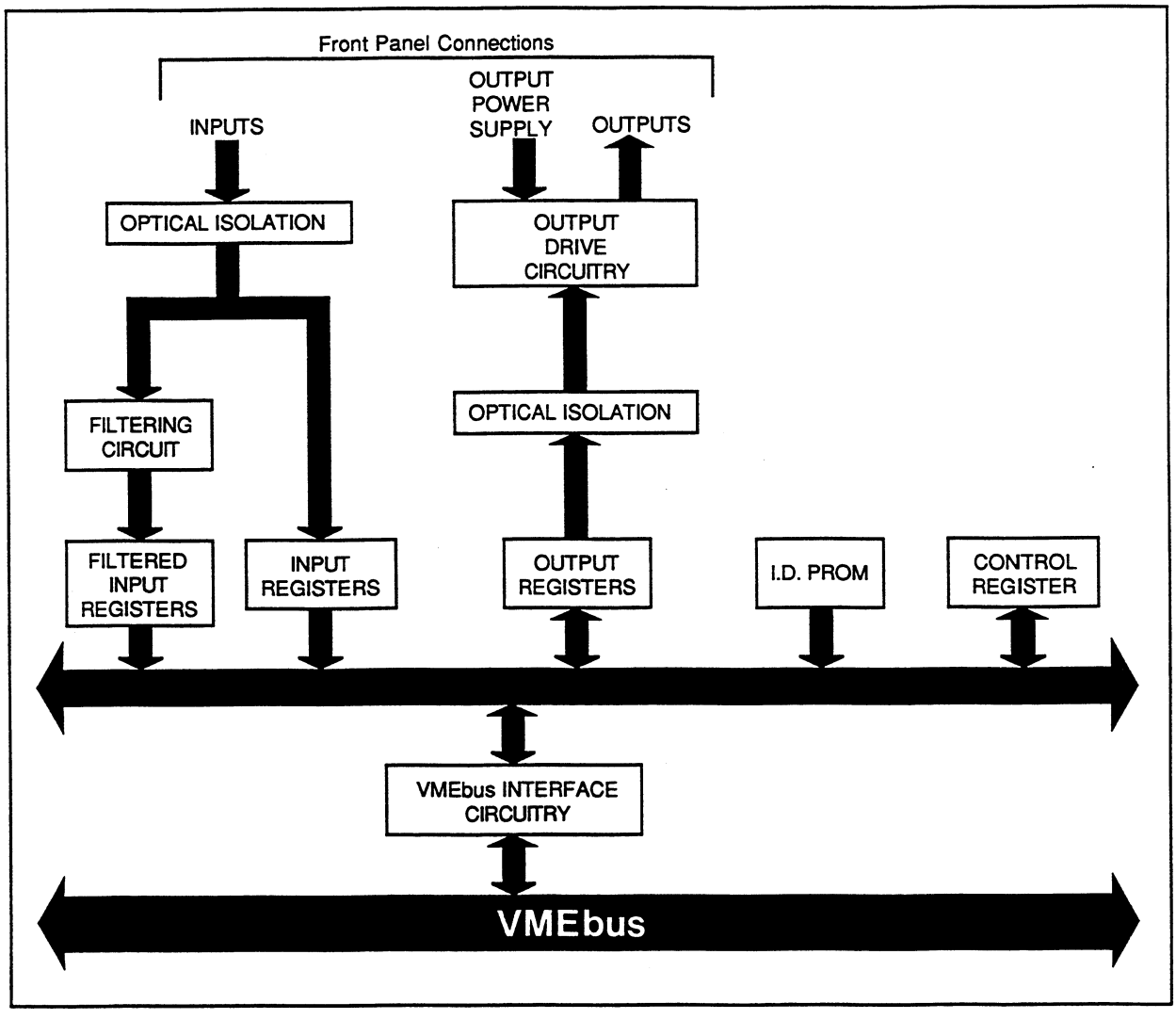


Figure B-1. XVME-244 Block Diagram

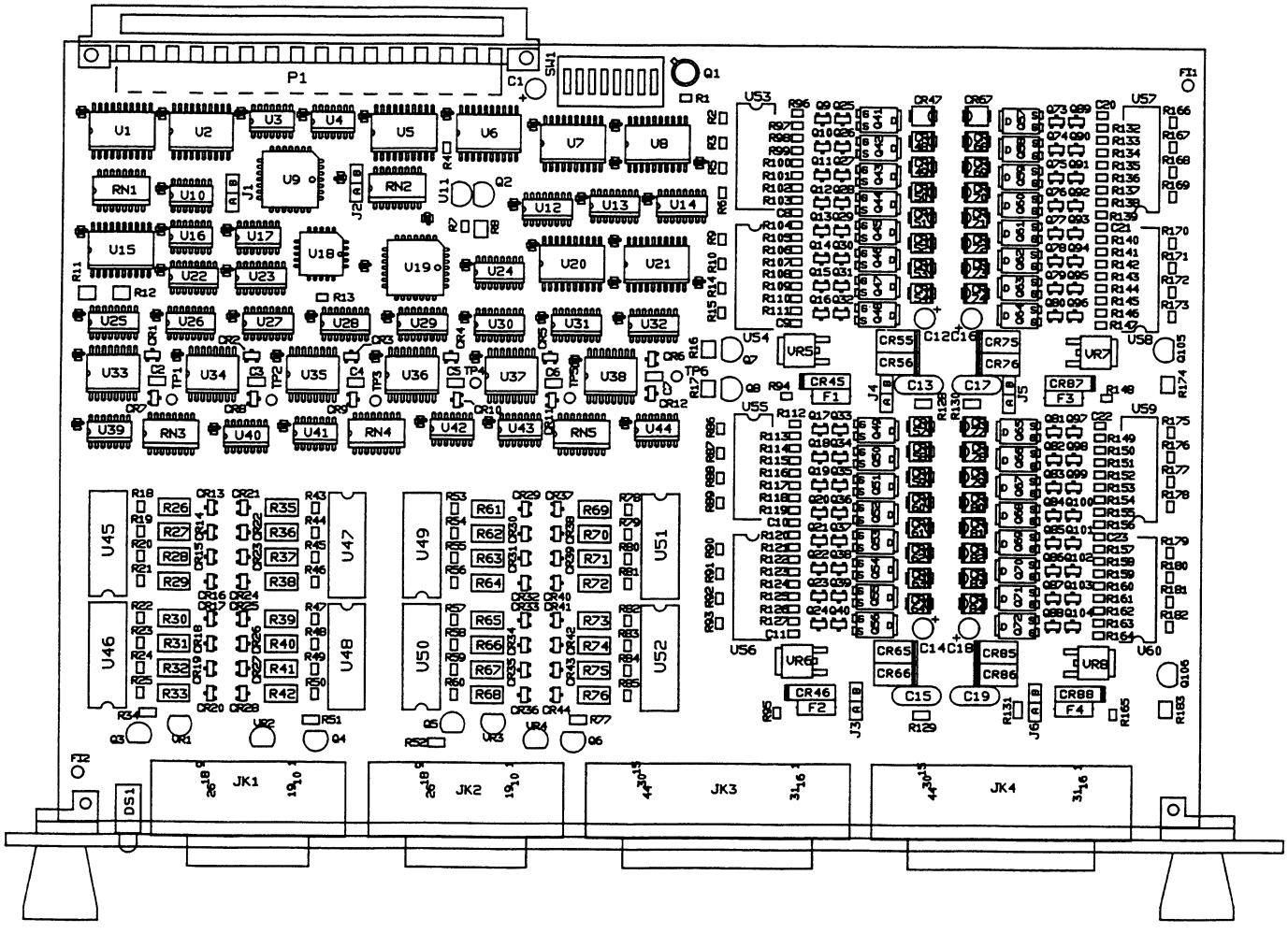
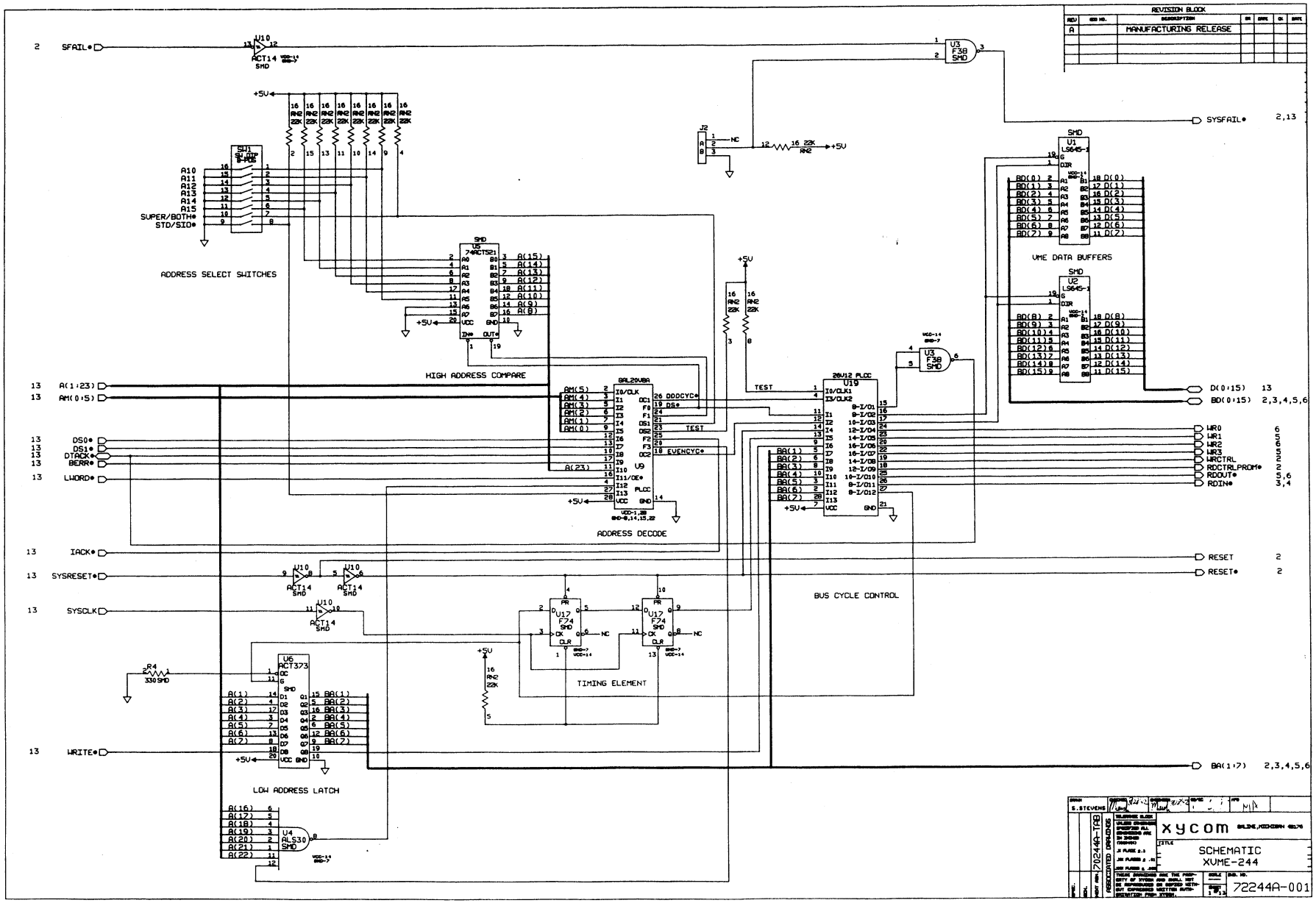
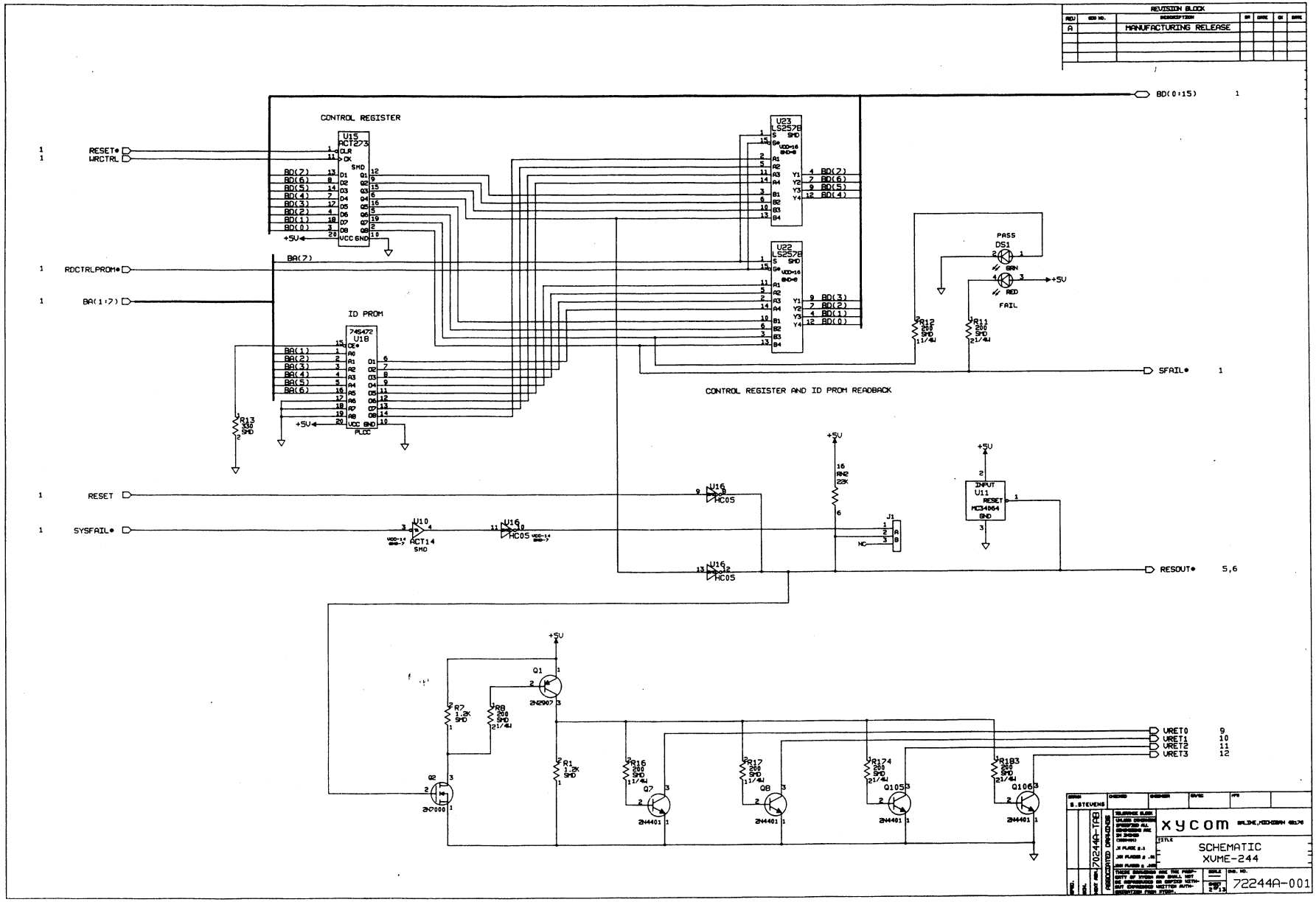


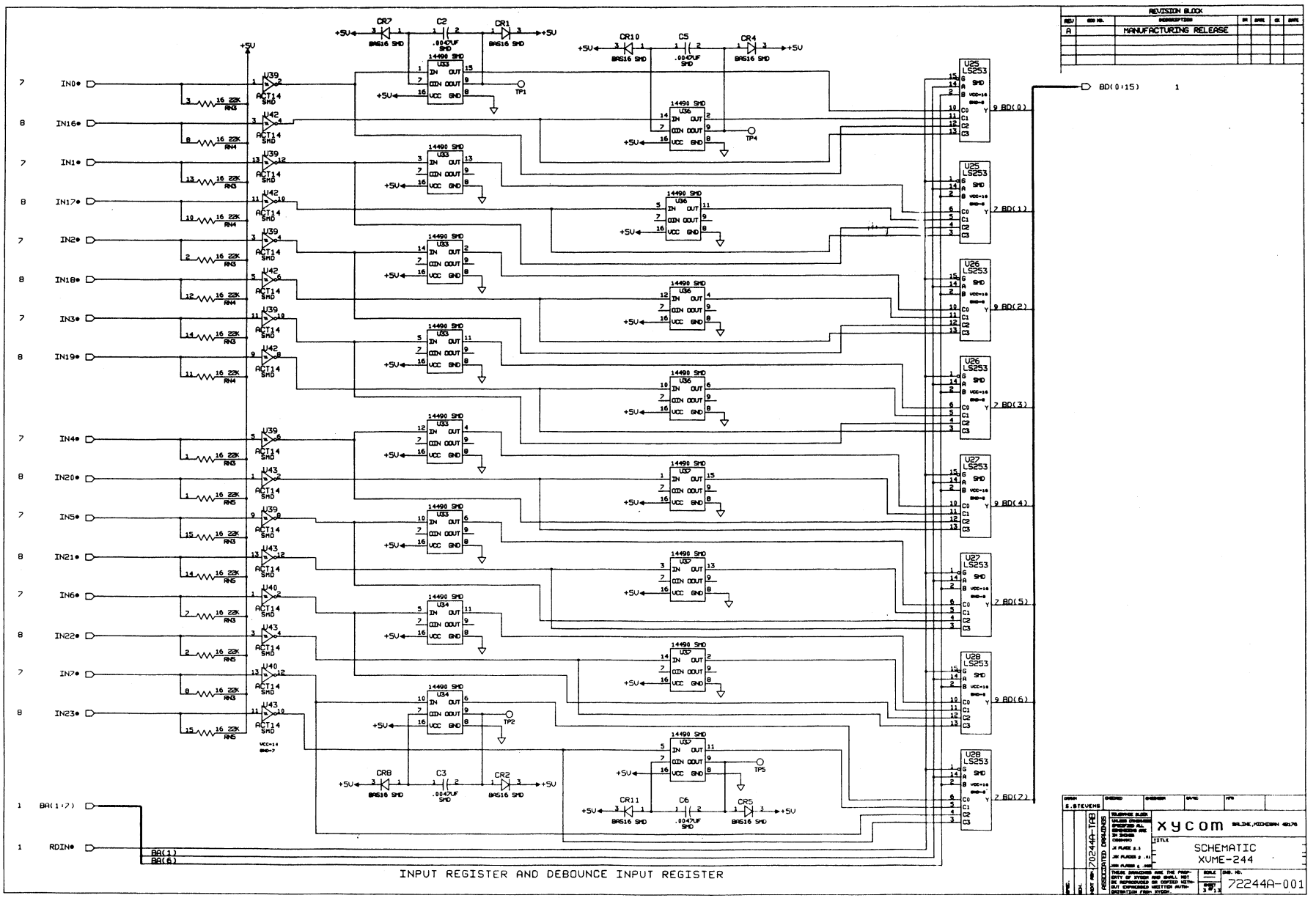
Figure B-2. XVME-244 Assembly Drawing



XVME-244 Schematic, Sheet 1 of 13



XVME-244 Schematic, Sheet 2 of 13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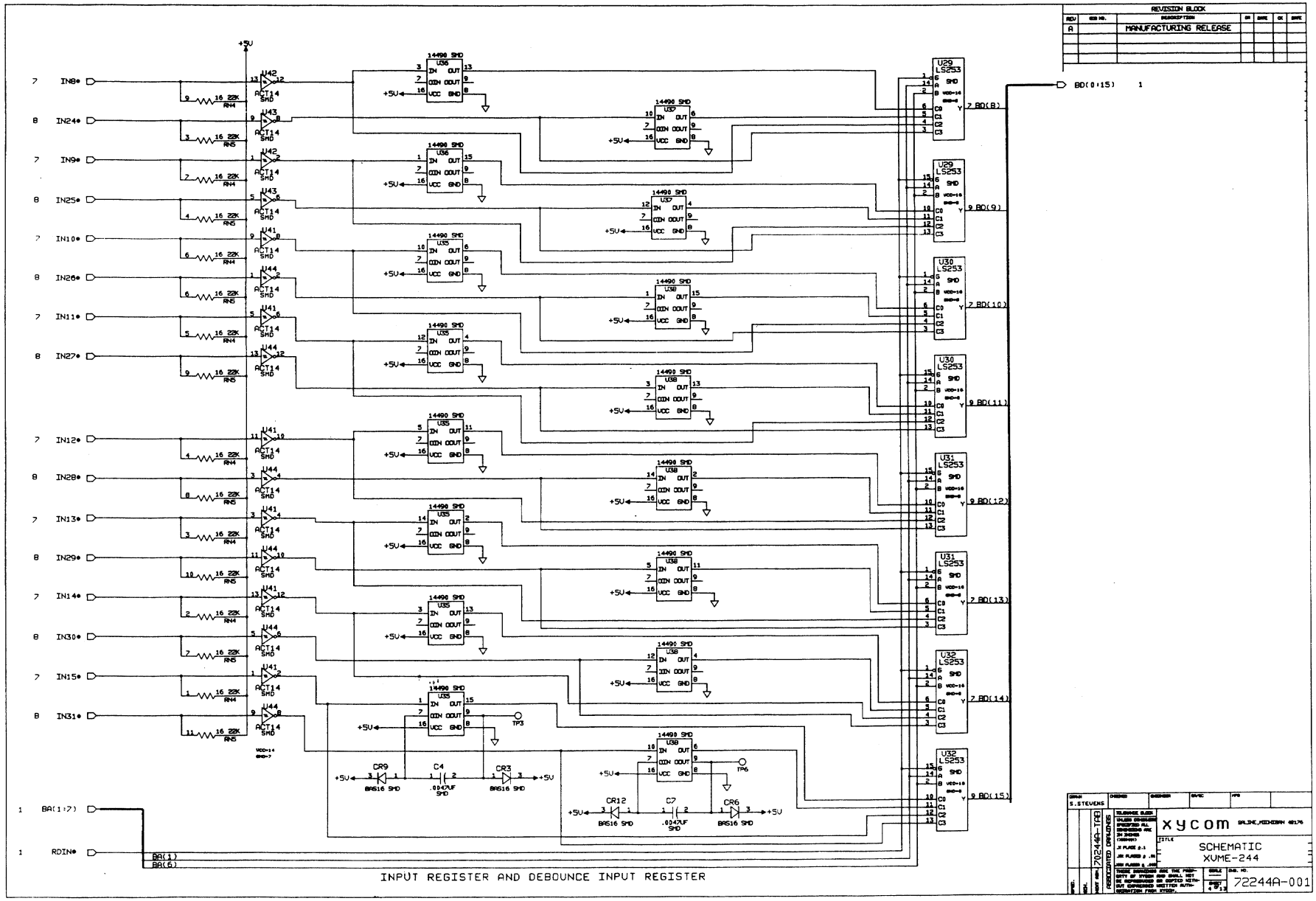
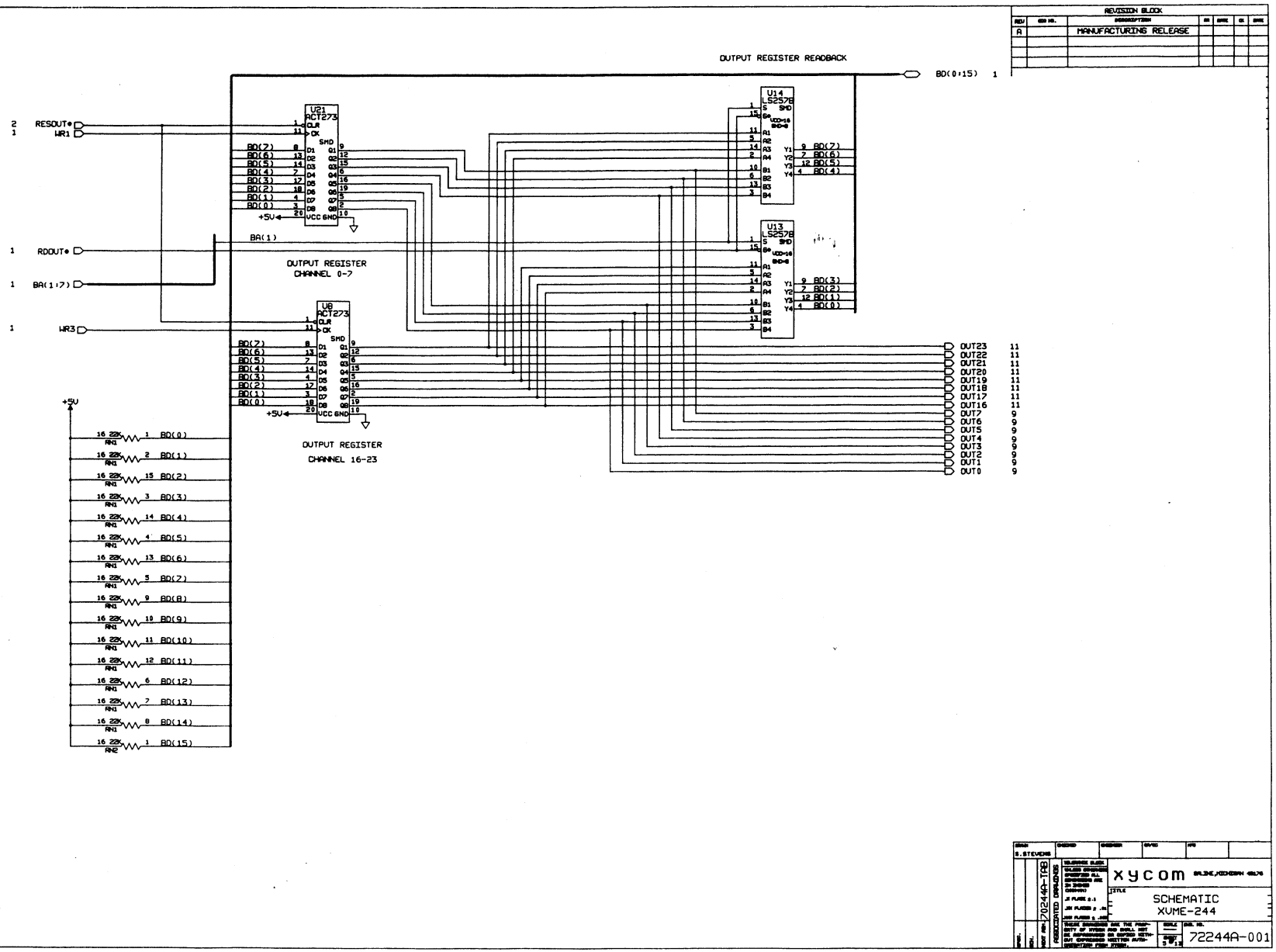
A MANUFACTURING RELEASE
INPUT REGISTER AND DEBOUNCE INPUT REGISTER
BD(0:15)
BA(1:7)
RDIN*
IN0* IN16* IN1* IN17* IN2* IN18* IN3* IN19*
IN4* IN20* IN5* IN21* IN6* IN22* IN7* IN23*
+5V
CR7 CR1 CR10 CR4 CR8 CR2 CR11 CR5
C2 C5 C3 C6
BAS16 SMD
.0047UF SMD
14490 SMD
TP1 TP2 TP4 TP5
16 22K RNS
ACT14 SMD
U25 LS253
U26 LS253
U27 LS253
U28 LS253
xycom
SCHEMATIC
XVME-244
72244A-001
72244A-TPB
S.STEVENS



XVME-244 Schematic, Sheet 4 of 13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REV
DESCRIPTION
A
MANUFACTURING RELEASE
OUTPUT REGISTER READBACK
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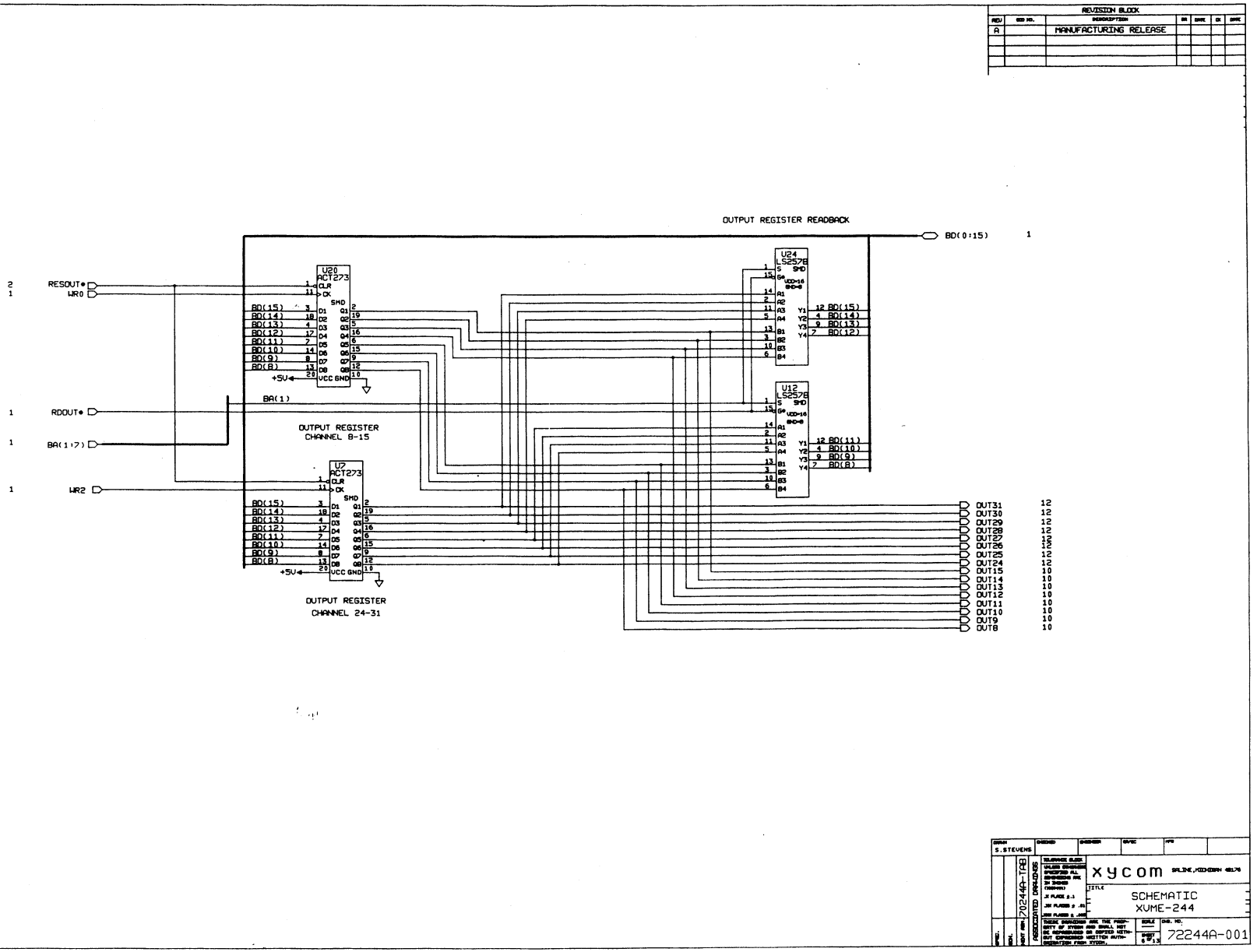
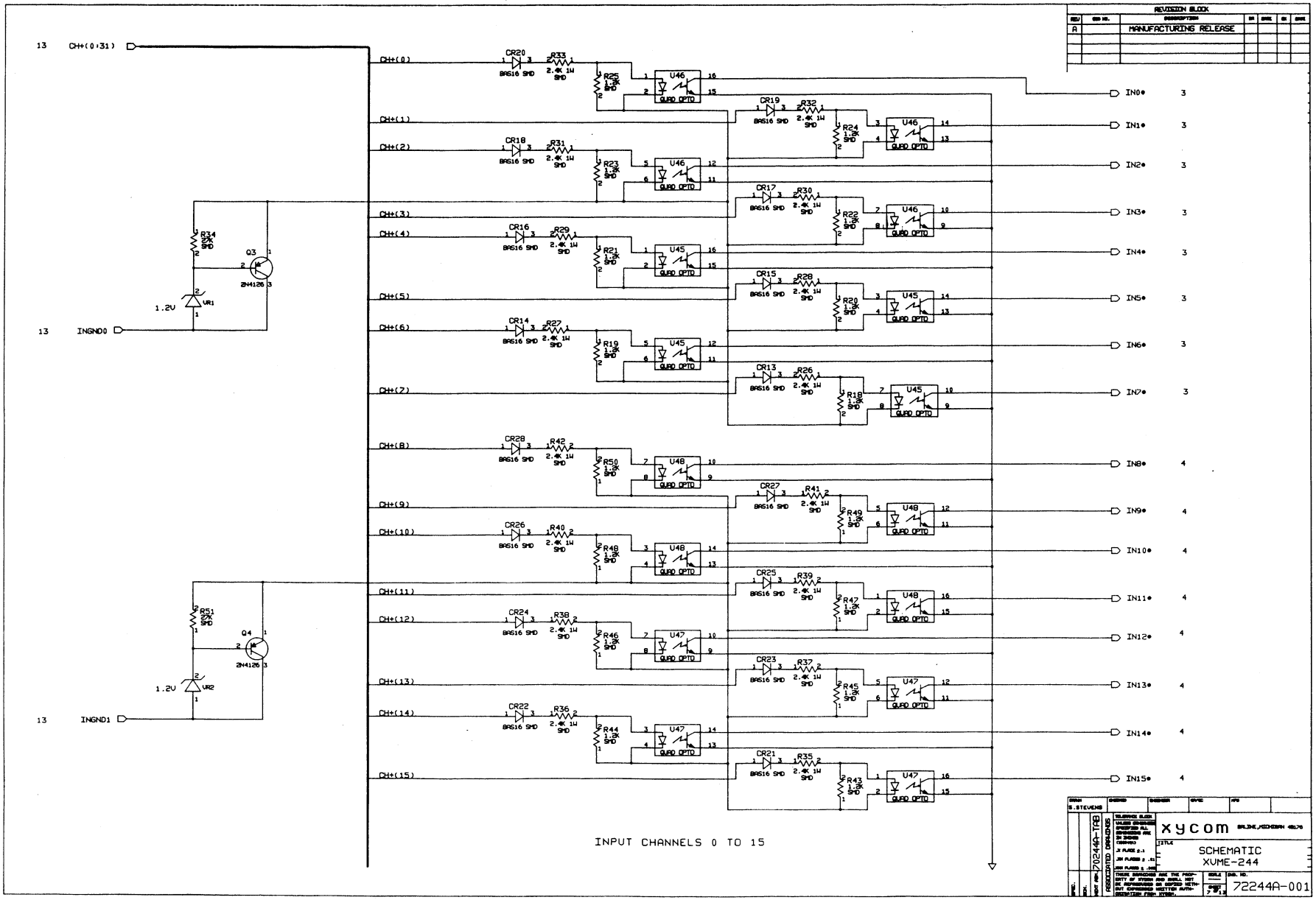
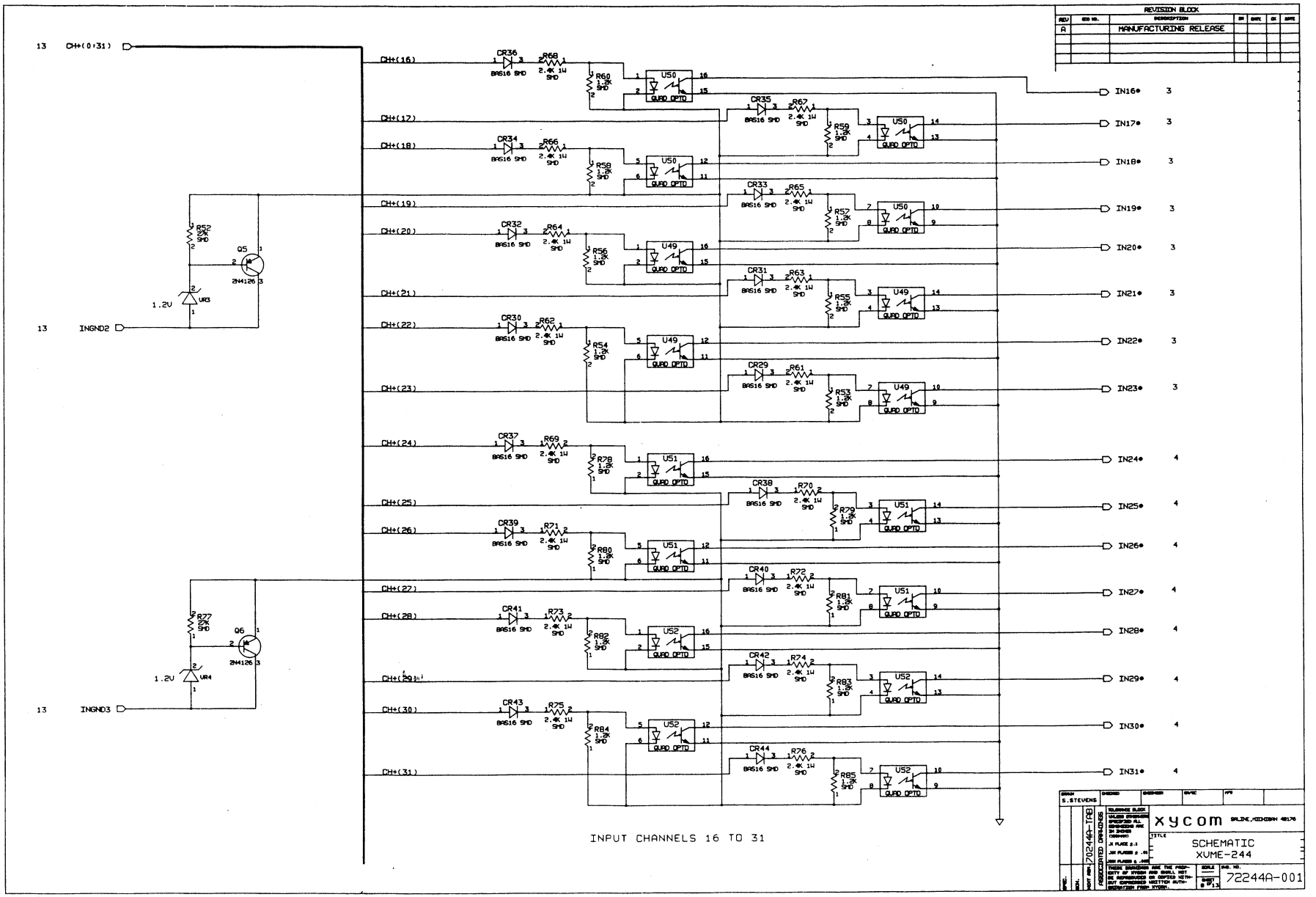
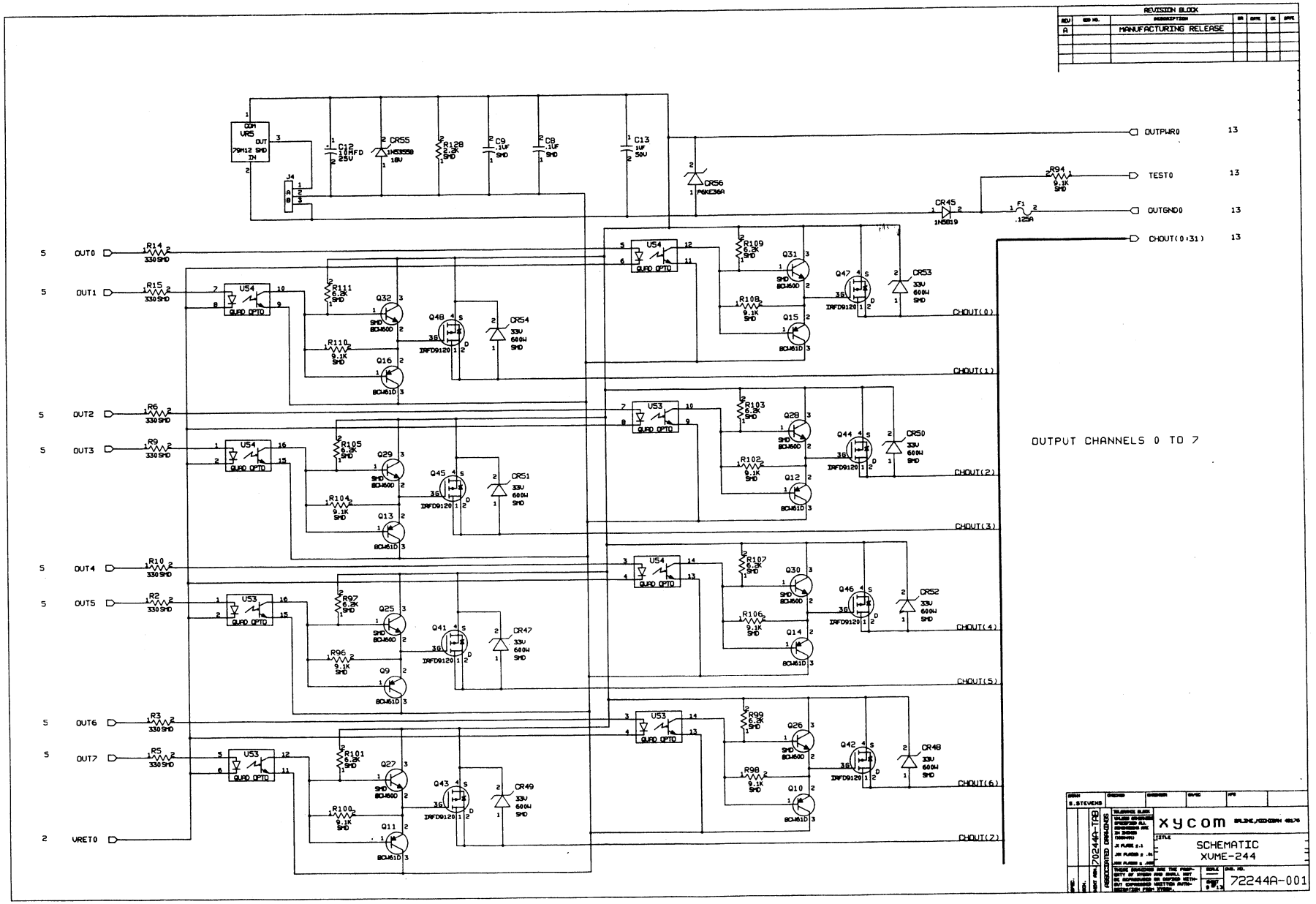
RESOUT*
WR1
RDOUT*
BA(1:7)
BA(1)
WR3
U21
ACT273
U8
ACT273
U14
LS257B
U13
LS257B
OUTPUT REGISTER
CHANNEL 0-7
OUTPUT REGISTER
CHANNEL 16-23
+5V
BD(0)
BD(1)
BD(2)
BD(3)
BD(4)
BD(5)
BD(6)
BD(7)
BD(8)
BD(9)
BD(10)
BD(11)
BD(12)
BD(13)
BD(14)
BD(15)
OUT23
OUT22
OUT21
OUT20
OUT19
OUT18
OUT17
OUT16
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT0
xycom
SCHEMATIC
XVME-244
72244A-001
72244A-TRB


REVISION BLOCK
A
MANUFACTURING RELEASE
OUTPUT REGISTER READBACK
BD(0:15)
RESOUT*
WR0
RDOUT*
BA(1:7)
WR2
BA(1)
U20
ACT273
U7
ACT273
U24
LS2578
U12
LS2578
OUTPUT REGISTER
CHANNEL 8-15
OUTPUT REGISTER
CHANNEL 24-31
OUT31
OUT30
OUT29
OUT28
OUT27
OUT26
OUT25
OUT24
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT8
S.STEVENS
xycom
SCHEMATIC
XVME-244
72244A-001
72244A-TAB


REVISION BLOCK
A
MANUFACTURING RELEASE
13 CH+(0:31)
13 INGND0
13 INGND1
1.2V
VR1
VR2
Q3
Q4
2N4126
R34 82K SMD
R51 82K SMD
CH+(0)
CH+(1)
CH+(2)
CH+(3)
CH+(4)
CH+(5)
CH+(6)
CH+(7)
CH+(8)
CH+(9)
CH+(10)
CH+(11)
CH+(12)
CH+(13)
CH+(14)
CH+(15)
CR20 BAS16 SMD
CR19 BAS16 SMD
CR18 BAS16 SMD
CR17 BAS16 SMD
CR16 BAS16 SMD
CR15 BAS16 SMD
CR14 BAS16 SMD
CR13 BAS16 SMD
CR28 BAS16 SMD
CR27 BAS16 SMD
CR26 BAS16 SMD
CR25 BAS16 SMD
CR24 BAS16 SMD
CR23 BAS16 SMD
CR22 BAS16 SMD
CR21 BAS16 SMD
R33 2.4K 1W SMD
R32 2.4K 1W SMD
R31 2.4K 1W SMD
R30 2.4K 1W SMD
R29 2.4K 1W SMD
R28 2.4K 1W SMD
R27 2.4K 1W SMD
R26 2.4K 1W SMD
R42 2.4K 1W SMD
R41 2.4K 1W SMD
R40 2.4K 1W SMD
R39 2.4K 1W SMD
R38 2.4K 1W SMD
R37 2.4K 1W SMD
R36 2.4K 1W SMD
R35 2.4K 1W SMD
R25 1.2K SMD
R24 1.2K SMD
R23 1.2K SMD
R22 1.2K SMD
R21 1.2K SMD
R20 1.2K SMD
R19 1.2K SMD
R18 1.2K SMD
R50 1.2K SMD
R49 1.2K SMD
R48 1.2K SMD
R47 1.2K SMD
R46 1.2K SMD
R45 1.2K SMD
R44 1.2K SMD
R43 1.2K SMD
U46 GUAD OPTO
U45 GUAD OPTO
U48 GUAD OPTO
U47 GUAD OPTO
IN0● 3
IN1● 3
IN2● 3
IN3● 3
IN4● 3
IN5● 3
IN6● 3
IN7● 3
IN8● 4
IN9● 4
IN10● 4
IN11● 4
IN12● 4
IN13● 4
IN14● 4
IN15● 4
INPUT CHANNELS 0 TO 15
S.STEVENS
xycom
SCHEMATIC
XVME-244
72244A-001
72244A-TAB



XVME-244 Schematic, Sheet 8 of 13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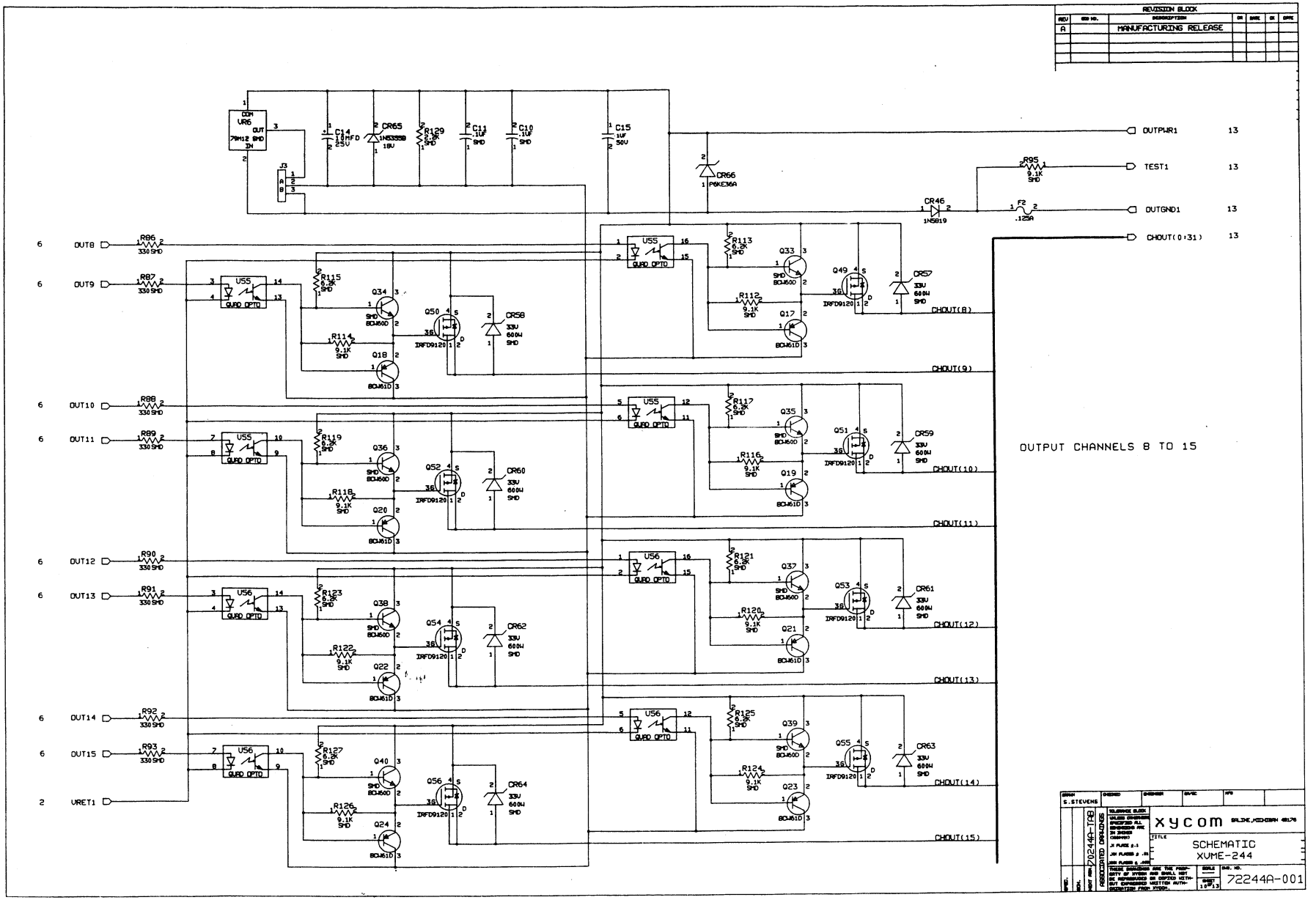
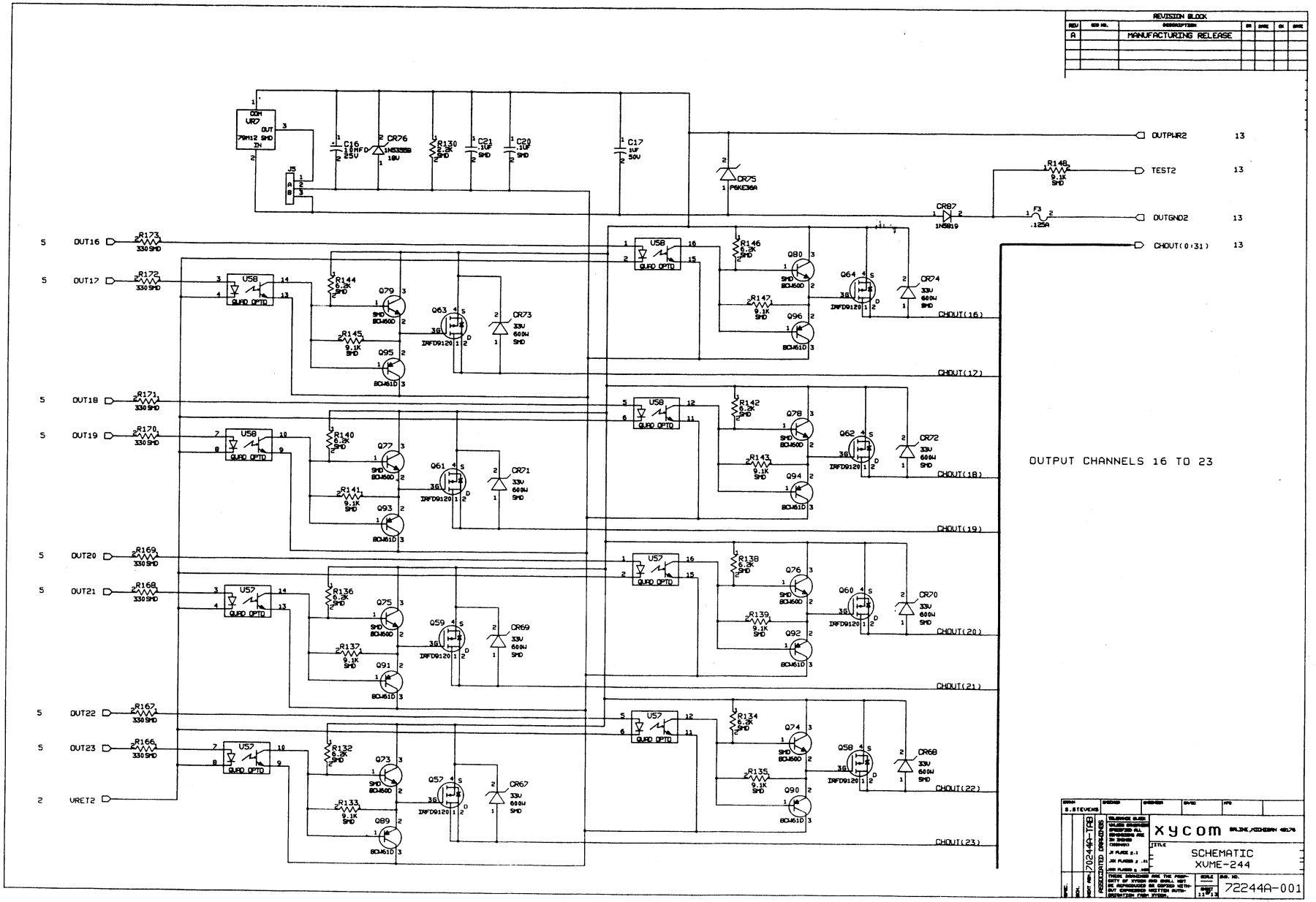
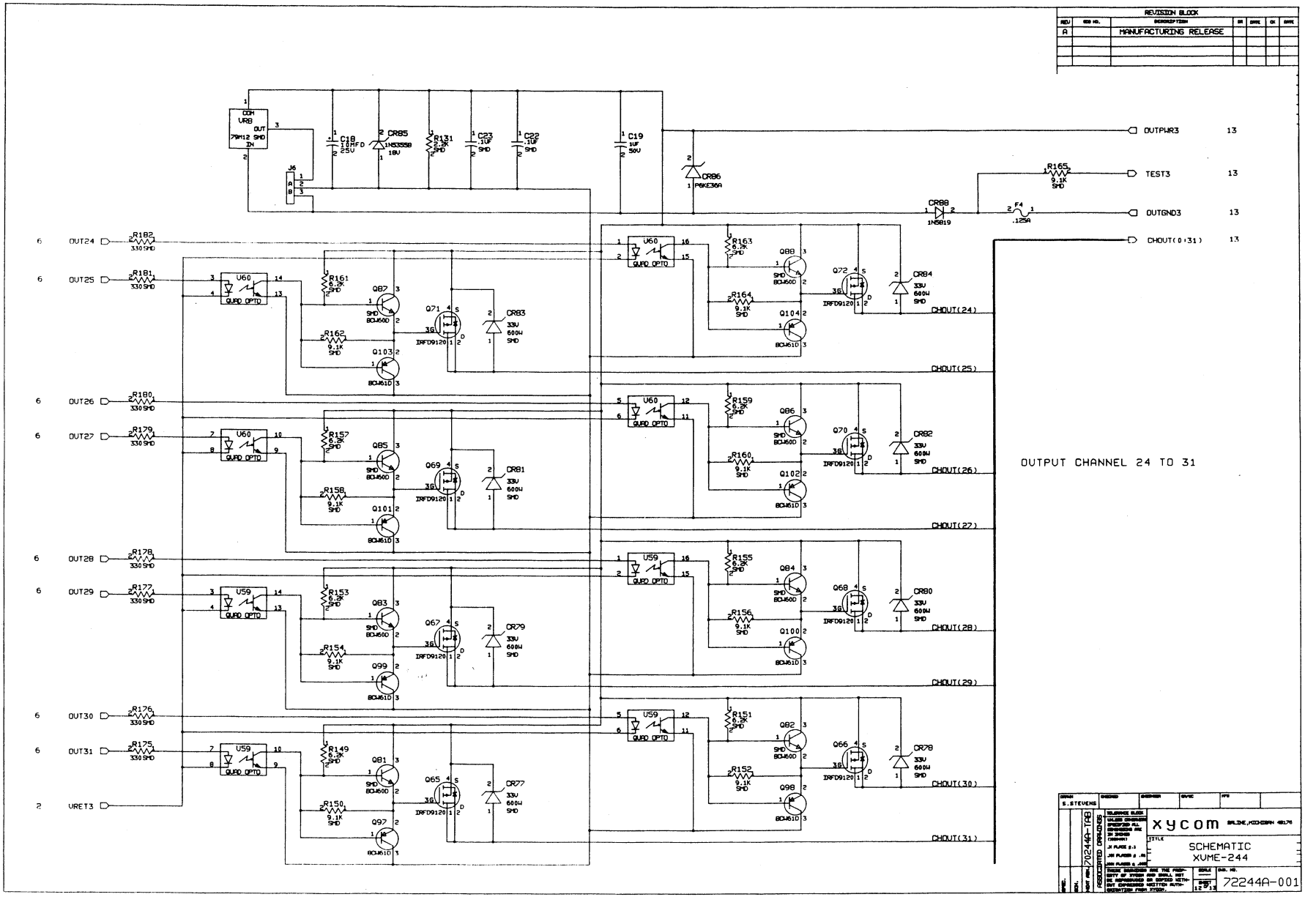
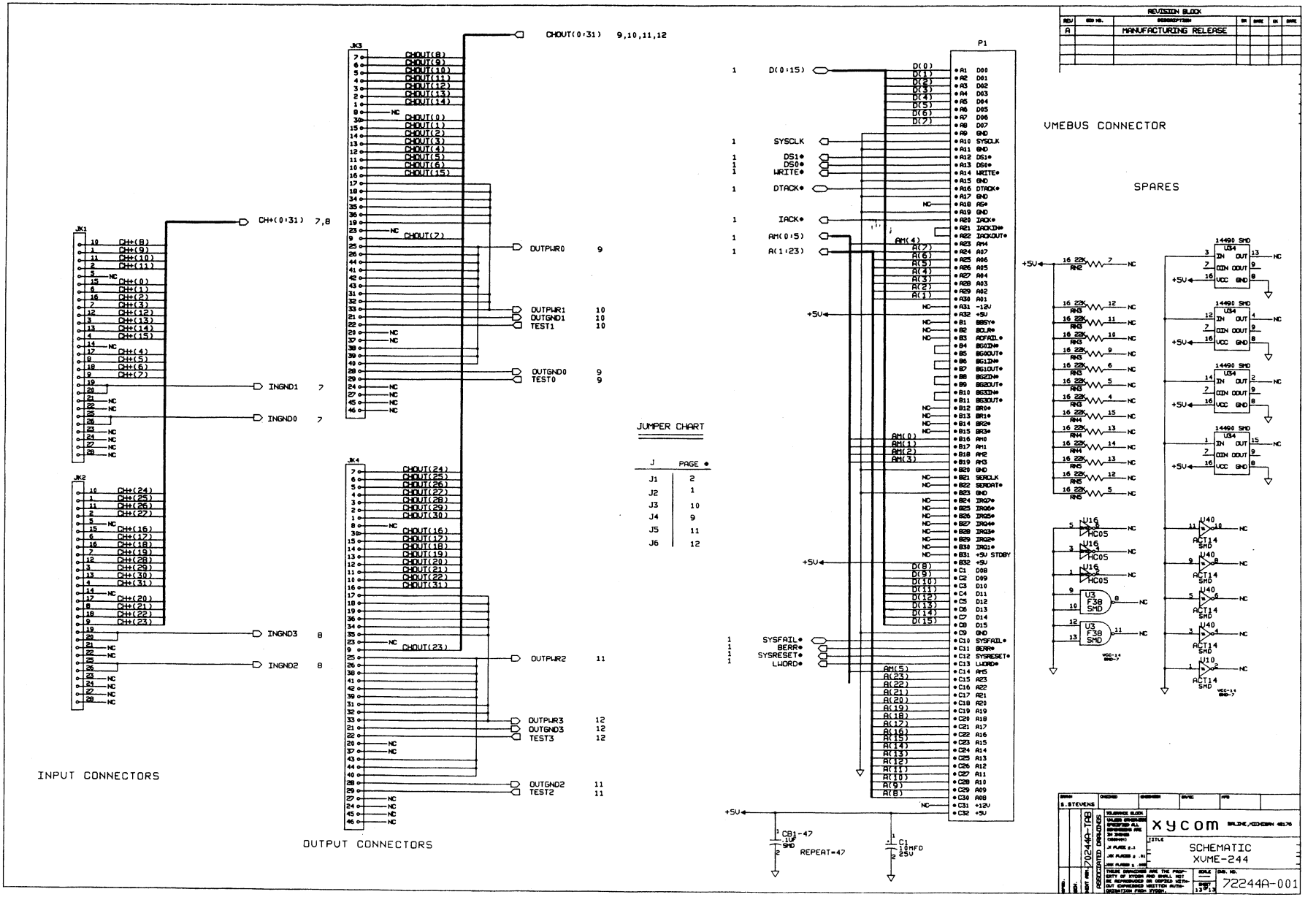
MANUFACTURING RELEASE
OUTPWR0
TEST0
OUTGND0
CHOUT(0:31)
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
VRET0
OUTPUT CHANNELS 0 TO 7
CHOUT(0)
CHOUT(1)
CHOUT(2)
CHOUT(3)
CHOUT(4)
CHOUT(5)
CHOUT(6)
CHOUT(7)
xycom
SCHEMATIC
XVME-244
72244A-001



XVME-244 Schematic, Sheet 10 of 13


REVISION BLOCK
REV
DESCRIPTION
A
MANUFACTURING RELEASE
OUTPWR2
TEST2
OUTGND2
CHOUT(0:31)
OUT16
OUT17
OUT18
OUT19
OUT20
OUT21
OUT22
OUT23
VRET2
CHOUT(16)
CHOUT(17)
CHOUT(18)
CHOUT(19)
CHOUT(20)
CHOUT(21)
CHOUT(22)
CHOUT(23)
OUTPUT CHANNELS 16 TO 23
U58
U57
QUAD OPTO
xycom
SCHEMATIC
XVME-244
72244A-001


REVISION BLOCK
A
MANUFACTURING RELEASE
OUTPUT CHANNEL 24 TO 31
OUTPWR3
TEST3
OUTGND3
CHOUT(0:31)
OUT24
OUT25
OUT26
OUT27
OUT28
OUT29
OUT30
OUT31
VRET3
CHOUT(24)
CHOUT(25)
CHOUT(26)
CHOUT(27)
CHOUT(28)
CHOUT(29)
CHOUT(30)
CHOUT(31)
xycom
SCHEMATIC
XVME-244
72244A-001


REVISION BLOCK
A MANUFACTURING RELEASE
VMEBUS CONNECTOR
SPARES
INPUT CONNECTORS
OUTPUT CONNECTORS
JUMPER CHART
J PAGE
J1 2
J2 1
J3 10
J4 9
J5 11
J6 12
P1
JK1
JK2
JK3
JK4
CHOUT(0:31) 9,10,11,12
CH+(0:31) 7,8
OUTPWR0 9
OUTPWR1 10
OUTGND1 10
TEST1 10
OUTGND0 9
TEST0 9
INGND1 7
INGND0 7
INGND3 8
INGND2 8
OUTPWR2 11
OUTPWR3 12
OUTGND3 12
TEST3 12
OUTGND2 11
TEST2 11
D(0:15)
SYSCLK
DS1*
DS0*
WRITE*
DTACK*
IACK*
AM(0:5)
A(1:23)
SYSFAIL*
BERR*
SYSRESET*
LWORD*
+5V
CB1-47
1UF
REPEAT=47
C1
10MFD
25V
XYCOM
SCHEMATIC
XVME-244
72244A-001

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